Document Title

A8137M0 Data Sheet, 2.4GHz FSK/GFSK 13dBm SoC

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue.	Aug. 2016	Objective
0.1	Revise pin configuration、pin description. update chapter 9 Revise chapter 22.4	Feb. 2017	Preliminary
0.2	update features, chapter 9,and pin descriptions,	Jun., 2017	Preliminary

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1. General Description

A8137M0 is a high performance and low cost 2.4GHz ISM band FSK/GFSK wireless SoC. It integrates M0 micro controller, 64KBytes flash memory, 8KBytes SRAM, Li-Ion battery charger and excellent performance of 2.4GHz RF transceiver.

For packet handling, A8137M0 has built-in separated 64-bytes TX/RX FIFO for data buffering and burst transmission, auto-ack and auto-resend, CRC for error packet filtering, FEC for 1-bit data correction per code word, RSSI for clear channel assessment, thermal sensor for monitoring relative temperature, WOR (Wake on RX) function to support periodically wake up from sleep mode to RX mode and listen for incoming packets without MCU interaction, data whitening for data encryption / decryption. Those functions are very easy to use while developing a wireless system.

2. Typical Applications

- Wireless sensor network
- 2.4GHz active RFID
- 2400 ~ 2483.5 MHz ISM system
- Smart remote controller
- Home and building automation
- Wireless toys and game controllers

3. Features

- Package size (QFN6 X6, 48 pins).
- Integrate M0 micro controller, 64KByte Flash memory with copy protection, 8KByte data RAM.
- In-Circuit Debugger.
- In-System programming/ In-Application programming.
- Operation clock: 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 of crystal oscillator.
- UART x3, I^2C x1, SPI x1, 32bit counter/timers x2, 32-bit dual MODE timer x1, PWM x8 and Watchdog timer.
- 24 GPIO and Key wake-up.
- Integrated RC Oscillator for Sleep timer and WOR /TWOR function.
- Support 2.4GHz FSK/GFSK modulation.
- TX current consumption (55 mA @ 13dBm).
- RX current consumption (21.5 mA).
- PM3 current (2.7 uA).
- Programmable TX power level up to 13 dBm.
- High sensitivity: -92dBm at 2Mbps on-air data rate.
- Fast settling time for frequency hopping system.
- On chip regulator, support input voltage 2.0 ~ 3.6 V.
- Support low cost crystal (16 MHz).
- Support RTC clock (32.768KHz).
- ONE register setting for new channel frequency.
- 8-bits Digital RSSI for clear channel indication.
- Auto Calibrations.
- Auto IF function.
- Clear channel assessment (CCA).
- Auto-ACK and Auto-resend scheme.
- Auto RSSI measurement.
- Auto CSMA-CA.
- Auto FCS (CRC) and Filtering.
- Separated 64 bytes FIFO for RX and TX.
- Support ED (Energy Detect) for CCA.
- Built-in Battery Detect, Thermal Sensor and Crystal load capacitors.
- Integrate charger for 4.2V Li-Ion battery.

4. Pin Configurations

Figure 4.1 A8137M0 QFN 6x6 48 pin Package Top View

5. Pin Descriptions (I: input; O: output, I/O: input or output)

Pin No.	Symbol	I/O	Function Description
1	TS	AI	Temperature sense input.
2	CHRG	DO	Charger state indicator.
3	VRCC	AO	Reference of charge current setting.
4	VRFL	AO	Reference of float voltage.
5	VDD_S	AO	VDD_S supply voltage output.
6	BG	AO	Band gap output.
7	VDD_R	AO	IF test pin
8	VDD_A	AO	VDD_A supply voltage output.
9	RFN	AIO	Negative RF IO.
10	RFP	AIO	Positive RF IO.
11	VDD_PA	AO	PA supply voltage output.
12	REGI_PA	AI	PA regulator input.
13	VDD_P	AO	PLL supply voltage output.
14	LPF	AO	PLL loop filter output.
15	XI	AI	Crystal oscillator input.
16	XO	AO	Crystal oscillator output.
17	REGI	AI	Regulator input.
18	VDD_D	AO	VDD_D supply voltage output.
19	VDD_FH	AO	Flash high voltage output.
20	P0.0	DIO	SPI_CS
21	P0.1	DIO	SPI_MISO
22	P0.2	DIO	SPI_MOSI
23	P0.3	DIO	SPI_SCK
24	P0.4	DIO	I^2CL
25	P0.5	DIO	I^2CD
26	P0.6	DIO	SWDIOTMS
27	P0.7	DIO	SWCLKTCK
28	P0.8	DIO/AI	Timer0_EIN/ADC2
29	P0.9	DIO/AI	Timer1_EIN/ADC3
30	P0.10	DIO	PWM2
31	P0.11	DIO	PWM3
32	P0.12	DIO/AI	PWM4/ADC4/ICE_MODE
33	P0.13	DIO/AI	PWM5/ADC5//BB_GIO1
34	P0.14	DIO/AI	PWM6/ADC6/BB_GIO2
35	P0.15	DIO/AI	PWM7/ADC7BB_CKO
36	P0.16	DIO	UART0_RX
37	P0.17	DIO	UART0_TX
38	P0.18	DIO/AI	UART1_RX/ADC0
39	P0.19	DIO/AI	UART1_TX/ADC1
40	P0.20	DIO	UART2_RX/PWM0.
41	P0.21	DIO	UART2_TX/PWM1.
42	P0.22	DIO/AI	RTCI
43	P0.23	DIO/AO	RTCO
44	RESETN	DI	RESETN input.
45	REGI	AI	Regulator input.
46	VCHRO	AO	Charger voltage output.
47	VBAT	AO	Charger current output.
48	VDD_C	AI	Charger supply voltage input.
	Back side plate	G	**Ground.** **Back side plate shall be well-solder to ground; otherwise, it will impact RF performance.**

Table 5.1 A8137M0 QFN6x6 48 pins

6. Chip Block Diagram

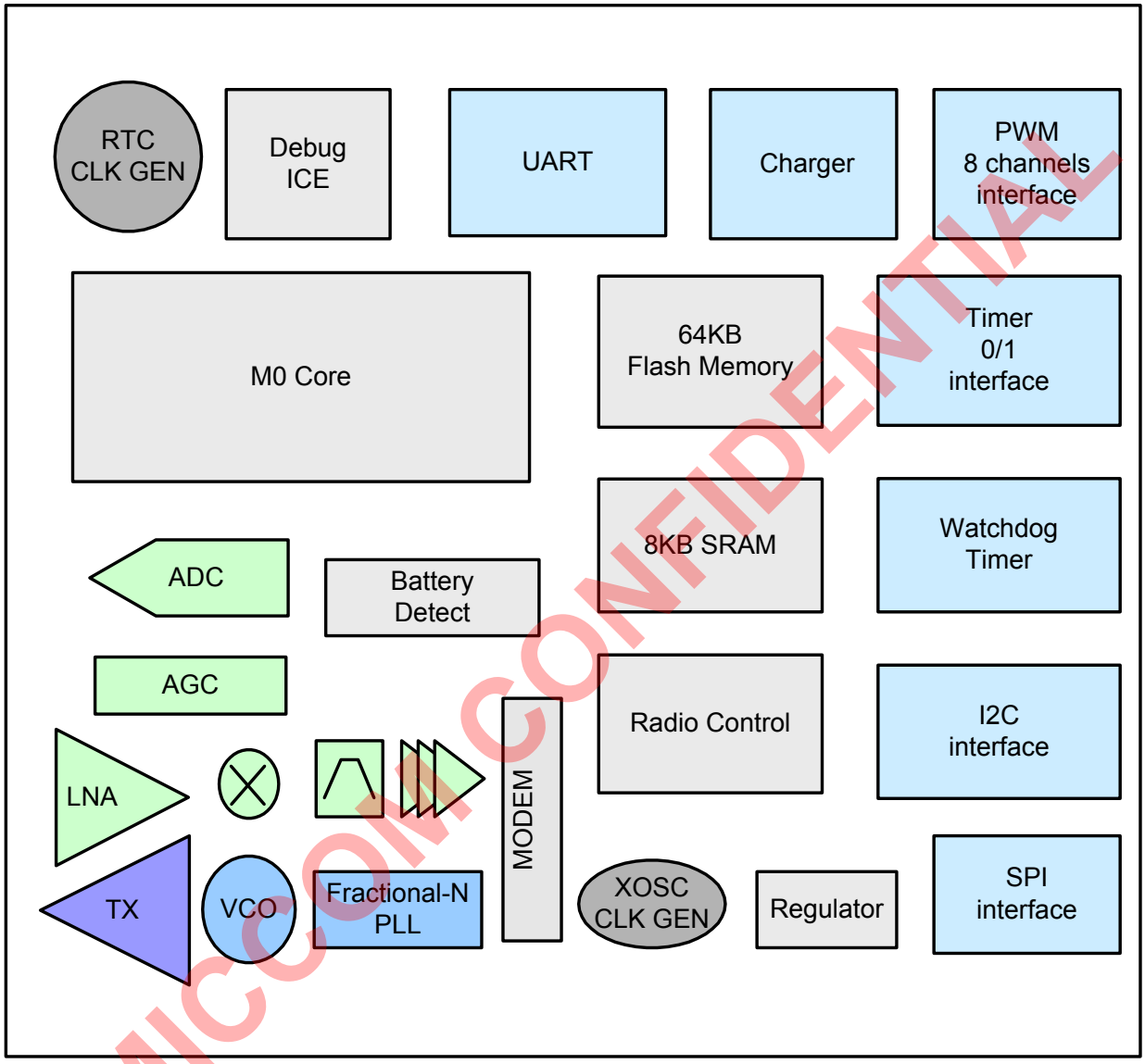


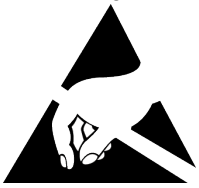
Figure 6.1 A8137M0 Block Diagram

7. Absolute Maximum Ratings

Parameter	With respect to	Rating	Unit
Supply voltage range (VDD_C)	GND	-0.3 ~ 6	V
Supply voltage range (VDD_IO)	GND	-0.3 ~ 3.6	V
Digital IO pins range	GND	-0.3 ~ VDD_IO+0.3	V
Voltage on the analog pins range	GND	-0.3 ~ 1.5	V
Input RF level		10	dBm
Storage Temperature range		-55 ~ 125	°C
ESD Rating	HBM	+/- 2KV*	V
	MM	+/- 100V*	V

*Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions. HBM (Human Body Mode) is tested under MIL-STD-883F Method 3015.7. MM (Machine Mode) is tested under JEDEC EIA/JESD22-A115-A.
*Device is Moisture Sensitivity Level III (MSL 3).
* RF PIN is HBM ± 1000V and MM ± 50V.



8. Electrical Specification

(Ta=25℃, VDD=3.3V, data rate= 2Mbps, F_{XTAL} =16MHz, On Chip Regulator = 1.2V, PN9 pattern, with matching network and low pass filter, unless otherwise noted.)

Parameter	Description	Min.	Typ.	Max.	Unit
General					
Operating Temperature		-40		85	℃
Supply Voltage (VDD_C)	Charger supply input	4.5	5	5.25	V
Supply Voltage (VDD_IO)	IO supply input	2.0	3.3	3.6	V
Current Consumption (MCU in stop mode and RF in sleep mode)	PM1 with sleep timer		4		uA
	PM2 with sleep timer		4		uA
	PM3 with sleep timer		3.1		uA
	PM3 without sleep timer		2.7		uA
Current Consumption (MCU in normal mode) MCU Clock @ 16MHz	Sleep Mode		3.5		mA
	Standby Mode		4		mA
	PLL Mode		9		mA
	RX Mode (AGC On)		21.5		mA
	TX Mode (@13dBm output)		55		mA
Synthesizer block					
Crystal settling Time	Idle to standby (XTAL 49US)		0.5		ms
Crystal frequency			16		MHz
Crystal tolerance			±20		ppm
Crystal Load Capacitance			18		pF
Crystal ESR				80	ohm
PLL settling Time	Standby to PLL		50		μs
Transmitter					
Carrier Frequency		2400		2483.5	MHz
Maximum Output Power			13		dBm
RF Power Control Range			25		dB
Out Band Spurious Emission	30MHz~1GHz			-36	dBm
	1GHz~12.75GHz			-30	
	1.8GHz~ 1.9GHz			-47	
	5.15GHz~ 5.3GHz			-47	
Data rate		1	2	2	Mbps
TX settling Time	PLL to TX		60		μs
Receiver					
Receiver sensitivity@ BER = 0.1%	2M mode		-92		dBm
IF Filter bandwidth	1Mbps		1.25		MHz
	2Mbps		2.50		MHz
IF center frequency	1Mbps		1		MHz
	2Mbps		2		MHz
Interference Channel space is 2MHz.	Co-Channel (C/Io)		11		dB
	1st Adjacent Channel (C/I_1)		2		dB
	2nd Adjacent Channel (C/I_2)		-18		dB
	3rd Adjacent Channel (C/I_3)		-28		dB
	Image (C/I_{IM})		-12		dB
Maximum Operating Input Power	@RF input (BER = 0.1%)			0	dBm
RX Spurious Emission	30MHz~1GHz			-57	dBm
	1GHz~12.75GHz			-47	

RSSI Range	@RF input	-100		-20	dBm
RX settling Time	PLL to RX		60		μs
SPI					
SCK period			4		MHz
MISO setup		10			ns
MISO hold		10			ns
12bit SAR ADC					
SAR Conversion clock rate			4		MHz
Conversion time in SAR clocks		20			clock
Input voltage range		0		0.6	V
Regulator					
Regulator settling time	Connected to 0.2uF		200		μs
Band-gap reference voltage			1.2		V
Regulator output voltage			1.2		V
Digital I/O DC characteristics					
High Level Input Voltage (V_{IH})		0.8*VDD		VDD	V
Low Level Input Voltage (V_{IL})		0		0.2*VDD	V
High Level Output Voltage (V_{OH})	@I_{OH}= -0.5mA	VDD-0.4		VDD	V
Source current	@VOH = 2.4V		8		mA
Low Level Output Voltage (V_{OL})	@I_{OL}= 0.5mA	0		0.4	V
Sink current	@VOL = 0.4V		5		mA
Charger					
Regulated output (float) voltage			4.2		V
Trickle charge threshold voltage			2.9		V
Recharge voltage			4.05		V
Under voltage			4.2		V
Trickle charge current			15		mA
BAT charge current			150		mA
Standby current			100		uA
Shutdown current			1		uA
CHG current	Weak pull down		20		uA
	Strong pull down		5		mA

9.Register List

A8137M0 contains Peripheral Register、RF Register and Power Control Register

9.1 RF Register Overview

RF control register start at Address[31:0]= 50010000

Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
Reset	0x0000	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W									RESETN	FWPRN	FRPRN	FIFORN	BFCRN			
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
Strobe Command	0x0004	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W									STRB7	STRB6	STRB5	STRB4	STRB3	STRB2	STRB1	STRB0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
Mode Control	0x0008	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W								LENS	FIFOSS		AIF	DFCD	DFCRC	FMT	FMS	
		R									FIFOSS		AIF	CD		FMT	FMS	
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
STATUS	0x0010	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W																
		R	FPEN			CSMAF	CCAF	FPF	FECF	CRCF	CER	XER	PLLER	TRSR	TRER	RFSTATE2	RFSTATE1	RFSTATE0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RF Interrupt	0x0014	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W									ISTRN						TWIS	FPFIS
		R									INT	INTF			IST3	IST2	IST1	IST0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
ID I	0x0018	W	ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16
		R	ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		R	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
ID II	0x001C	W	ID63	ID62	ID61	ID60	ID59	ID58	ID57	ID56	ID55	ID54	ID53	ID52	ID51	ID50	ID49	ID48
		R	ID63	ID62	ID61	ID60	ID59	ID58	ID57	ID56	ID55	ID54	ID53	ID52	ID51	ID50	ID49	ID48
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40	ID39	ID38	ID37	ID36	ID35	ID34	ID33	ID32
		R	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40	ID39	ID38	ID37	ID36	ID35	ID34	ID33	ID32
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
FIFO Control	0x0020	W	FPM1	FPM0														
		R	FPM1	FPM0														
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W									PHR7	PHR6	PHR5	PHR4	PHR3	PHR2	PHR1	PHR0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
Data Rate	0x0024	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W									SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
		R									SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RF GIO	0x0028	W										CKOI				CKOS2	CKOS1	CKOS0
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0

		W		GIO2I			GIO2S3	GIO2S2	GIO2S1	GIO2S0		GIO1I			GIO1S3	GIO1S2	GIO1S1	GIO1S0
		R														P_IRQ2O	P_IRQ1O	P_CKO
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
Calibration	0x0080	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W												RSSC	VDC	VCC	VBC	FBC
		R												RSSC	VDC	VCC	VBC	FBC
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
IF Control	0x0084	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W											IFAS	MFBS	MFB3	MFB2	MFB1	MFB0
		R				FCD4	FCD3	FCD2	FCD1	FCD0			IFAS	FBCF	FB3	FB2	FB1	FB0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
VCO Current	0x0088	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W							PKT1	PKT0	PKTH	PKS	VCCS	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
		R												FVCC	VCB3	VCB2	VCB1	VCB0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
VCO band	0x008C	W								MDAGS	MDAG7	MDAG6	MDAG5	MDAG4	MDAG3	MDAG2	MDAG1	MDAG0
		R									ADAG7	ADAG6	ADAG5	ADAG4	ADAG3	ADAG2	ADAG1	ADAG0
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W												MVBS	MVB3	MVB2	MVB1	MVB0
		R												VBCF	VB3	VB2	VB1	VB0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
VCO Deviation	0x0090	W															CSW	DEVCM
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W									VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
		R									VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
VCO Deviation II	0x0094	W									MVDS	MDEV6	MDEV5	MDEV4	MDEV3	MDEV2	MDEV1	MDEV0
		R									ADEV7	ADEV6	ADEV5	ADEV4	ADEV3	ADEV2	ADEV1	ADEV0
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W									DEVS3	DEVS2	DEVS1	DEVS0	DAMR_M	VMTE_M	VMS_M	MSEL
		R									DEVA7	DEVA6	DEVA5	DEVA4	DEVA3	DEVA2	DEVA1	DEVA0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
Channel	0x00C0	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W									CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
		R									CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
Radio Frequency I	0x00C4	W								BIP8	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
		R								IP8	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
		R	--	AC14	AC13	AC12	AC11	AC10	AC9	AC8	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
Radio Frequency II	0x00C8	W									CHI3	CHI2	CHI1	CHI0	CHD3	CHD2	CHD1	CHD0
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W		CHR14	CHR13	CHR12	CHR11	CHR10	CHR9	CHR8	CHR7	CHR6	CHR5	CHR4	CHR3	CHR2	CHR1	CHR0
		R		CHR14	CHR13	CHR12	CHR11	CHR10	CHR9	CHR8	CHR7	CHR6	CHR5	CHR4	CHR3	CHR2	CHR1	CHR0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
Channel Group	0x00CC	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
		R	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16

TX Control	0x0100	W														FPS2	FPS1	FPS0
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W									PPS	TCPS	DEVSUB	GDR	FS	TXDI	TMDE	TME
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
TX Gain	0x0104	W	IBPAS	VBPAS	PGV_PA1	PGC_PA0	PA_TX1											
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W					PAV1	PAV0	PAB_HCS	PA_HCS	PWORS	TXCS	PAC2	PAC1	PAC0	TBG2	TBG1	TBG0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
TX Power	0x0108	W						RAMP2	RAMP1	RAMP0								
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W												TXUDS1	TXUDS0	TRT2	TRT1	TRT0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
TX Modulation	0x010C	W	XDS				DEVDS	DAMV1	DAMV0	DEVFD2	DEVFD1	DEVFD0	DEVD2	DEVD1	DEVD0	DEVGD2	DEVGD1	DEVGD0
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W						FDP2	FDP1	FDP0	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RX	0x0140	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W														RXDI	DMG	ULS
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RX Gain I	0x0144	W								IFPK	PKIS1	PKIS0	VTHS2	VTHS1	VTHS0	VTLS2	VTLS1	VTLS0
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W											IGS1	IGS0	MGS1	MGS0	LGS1	LGS0
		R							VTB1	VTB0			IGS1	IGS0	MGS1	MGS0	LGS1	LGS0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RX Gain II	0x0148	W										MHC3	MHC2	MHC1	MHC0	LHC2	LHC1	LHC0
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W												AGCS1	AGCS0	AGCKS1	AGCKS0	AGCE
		R																AGCE
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RX DEM I	0x0150	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W										DCKS	RCP2	RCP1	RCP0	SLF2	SLF1	SLF0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RX DEM II	0x0154	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W							DCM1	DCM0	DCV7	DCV7	DCV7	DCV7	DCV7	DCV7	DCV7	DCV7
		R							DCM1	DCM0	DCO7	DCO6	DCO5	DCO4	DCO3	DCO2	DCO1	DCO0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
CODE I	0x0180	W										ETH2	ETH1	ETH0	PTH2	PTH1	PTH0	IDL
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W													CRCIV	WHTS	FECS	CRCS
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
CODE II	0x0184	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W										WS6	WS5	WS4	WS3	WS2	WS1	WS0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
CODE	0x0188	W																

III		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	CRCPL15	CRCPL14	CRCPL13	CRCPL12	CRCPL11	CRCPL10	CRCPL9	CRCPL8	CRCPL7	CRCPL6	CRCPL5	CRCPL4	CRCPL3	CRCPL2	CRCPL1	CRCPL0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
CODE IV	0x018C	W	CRCTIV15	CRCTIV14	CRCTIV13	CRCTIV12	CRCTIV11	CRCTIV10	CRCTIV9	CRCTIV8	CRCTIV7	CRCTIV6	CRCTIV5	CRCTIV4	CRCTIV3	CRCTIV2	CRCTIV1	CRCTIV0
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	CRCRIV15	CRCRIV14	CRCRIV13	CRCRIV12	CRCRIV11	CRCRIV10	CRCRIV9	CRCRIV8	CRCRIV7	CRCRIV6	CRCRIV5	CRCRIV4	CRCRIV3	CRCRIV2	CRCRIV1	CRCRIV0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
Delay	0x01C0	W					PTRS3	PTRS2	PTRS1	PTRS0	WSEL2	WSEL1	WSEL0	AGC_D1	AGC_D0		RS_DLY1	RS_DLY0
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W									PADL		TDL2	TDL1	TDL0		PDL1	PDL0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RF Clock Control I	0x01C4	W								RDU	CGC1	CGC0	CGS		XCP	XCC	XS	XEC
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W								HFR	CGFS1	CGFS0	MDR1	MDR0	GRC3	GRC2	GRC1	GRC0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RF Clock Control II	0x01C8	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W											PRIC1	PRIC0	PRRC1	PRRC0	SDPW	NSDO
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
Charge Pump	0x01D0	W																CPS
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W							CPCH1	CPCH0	CPM3	CPM2	CPM1	CPM0	CPT3	CPT2	CPT1	CPT0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RF Test I	0x01D4	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W											CSXTL5	CSXTL4	CSXTL3	CSXTL2	CSXTL1	CSXTL0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RF Test II	0x01D8	W									FGC1	FGC0	CTR5	CTR4	CTR3	CTR2	CTR1	CTR0
		R									FGCR1	FGCR0	CTRR5	CTRR4	CTRR3	CTRR2	CTRR1	CTRR0
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W			BDC5	BDC4	BDC3	BDC2	BDC1	BDC0			STM5	STM4	STM3	STM2	STM1	STM0
		R											STMR5	STMR4	STMR3	STMR2	STMR1	STMR0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RF Test III	0x01DC	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W						INTPRC	VRPL1	VRPL0	VTRB3	VTRB2	VTRB1	VTRB0	VMRB3	VMRB2	VMRB1	VMRB0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
IF Test I	0x01E0	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	PRS	QLIM	LOVRS	LNAVRS	TLB1	TLB0	RLB1	RLB0	TXLO_HC	RXLO_HC	VCBS1	VCBS0	IFBC1	IFBC0	LIMC	IFAS
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
IF Test II	0x01E4	W											IFFATS	IFTS	ATP3	ATP2	ATP1	ATP0
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W																TRDC

		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
WOR & WOT I	0x0200	W																RNTWUNF
		R																TWUNF
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W			WUS1	WUS0	WTLP3	WTLP2	WTLP1	WTLP0						WORE	WOTE	TWWS
		R														WORE	WOTE	
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
WOR & WOT II	0x0204	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	RBTO15	RBTO14	RBTO13	RBTO12	RBTO11	RBTO10	RBTO9	RBTO8	RBTO7	RBTO6	RBTO5	RBTO4	RBTO3	RBTO2	RBTO1	RBTO0
		R	RBTD15	RBTD14	RBTD13	RBTD12	RBTD11	RBTD10	RBTD9	RBTD8	RBTD7	RBTD6	RBTD5	RBTD4	RBTD3	RBTD2	RBTD1	RBTD0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
WOR & WOT III	0x0208	W									RBT23	RBT22	RBT21	RBT20	RBT19	RBT18	RBT17	RBT16
		R									BFCNT23	BFCNT22	BFCNT21	BFCNT20	BFCNT19	BFCNT18	BFCNT17	BFCNT16
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	RBT15	RBT14	RBT13	RBT12	RBT11	RBT10	RBT9	RBT8	RBT7	RBT6	RBT5	RBT4	RBT3	RBT2	RBT1	RBT0
		R	BFCNT15	BFCNT14	BFCNT13	BFCNT12	BFCNT11	BFCNT10	BFCNT9	BFCNT8	BFCNT7	BFCNT6	BFCNT5	BFCNT4	BFCNT3	BFCNT2	BFCNT1	BFCNT0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
8 BIT ADC Control	0x0240	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W									ADCC	ADCOM1	ADCOM0	AVGS1	AVGS0	ARSSI	CDM	ADCM
		R									ADCC	ADCOM1	ADCOM0	AVGS1	AVGS0	ARSSI	CDM	ADCM
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
8 BIT threshold	0x0244	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W									CDTH7	CDTH6	CDTH5	CDTH4	CDTH3	CDTH2	CDTH1	CDTH0
		R									ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
8 BIT ADC CAL	0x0248	W																
		R	ADH7	ADH6	ADH5	ADH4	ADH3	ADH2	ADH1	ADH0	ADL7	ADL6	ADL5	ADL4	ADL3	ADL2	ADL1	ADL0
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W			CRS2	CRS1	CRS0	SRS2	SRS1	SRS0	MRHL	RSSL6	RSSL5	RSSL4	RSSL3	RSSL2	RSSL1	RSSL0
		R	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RF4CE Mode select	0x0300	W												CCAM1	CCAM0	SLT2	SLT1	SLT0
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	FMSS						ERX	EDS	CCAS		LQIS	ACKS	ARTS	CSMAS	SLOT	DLS
		R								EDS	CCAS							
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RF4CE CSMA-CA	0x0304	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W			CST1	CST0		MaxNB2	MaxNB1	MaxNB0	MaxBE3	MaxBE2	MaxBE1	MaxBE0	MinBE3	MinBE2	MinBE1	MinBE0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RF4CE ART	0x0308	W														ATLP2	ATLP1	ATLP0
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	RTRTD3	RTRTD2	RTRTD1	RTRTD0	RTTRD3	RTTRD2	RTTRD1	RTTRD0	RTRAT7	RTRAT6	RTRAT5	RTRAT4	RTRAT3	RTRAT2	RTRAT1	RTRAT0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RF4CE ACK	0x030C	W													ACKD3	ACKD2	ACKD1	ACKD0
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	AFCF15	AFCF14	AFCF13	AFCF12	AFCF11	AFCF10	AFCF9	AFCF8	AFCF7	AFCF6	AFCF5	AFCF4	AFCF3	AFCF2	AFCF1	AFCF0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RF4CE LQI	0x0310	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0

		W																LQICE
		R									LQIV7	LQIV6	LQIV5	LQIV4	LQIV3	LQIV2	LQIV1	LQIV0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RF4CE ADFC	0x0314	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	FADDE	ACBEN	ACDAT	ACACK	ACCMD	ACRES	PCORR	RESMU X2	RESMU X1	RESMU X0	MAXVE R1	MAXVE R0	MBEN			
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RF4CE PID	0x0318	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RF4CE SADD	0x031C	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	SADD15	SADD14	SADD13	SADD12	SADD11	SADD10	SADD9	SADD8	SADD7	SADD6	SADD5	SADD4	SADD3	SADD2	SADD1	SADD0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RF4CE LADD1	0x0320	W	LADD63	LADD62	LADD61	LADD60	LADD59	LADD58	LADD57	LADD56	LADD55	LADD5 4	LADD5 3	LADD5 2	LADD5 1	LADD50	LADD49	LADD48
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	LADD47	LADD46	LADD45	LADD44	LADD43	LADD42	LADD41	LADD40	LADD39	LADD3 8	LADD3 7	LADD3 6	LADD3 5	LADD34	LADD33	LADD32
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RF4CE LADD2	0x0324	W	LADD31	LADD30	LADD29	LADD28	LADD27	LADD26	LADD25	LADD24	LADD23	LADD2 2	LADD2 1	LADD2 0	LADD1 9	LADD18	LADD17	LADD16
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	LADD15	LADD14	LADD13	LADD12	LADD11	LADD10	LADD9	LADD8	LADD7	LADD6	LADD5	LADD4	LADD3	LADD2	LADD1	LADD0
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RF4CE PNG	0x0328	W															PNS	PNIVS
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	PNIV15	PNIV14	PNIV13	PNIV12	PNIV11	PNIV10	PNIV9	PNIV8	PNIV7	PNIV6	PNIV5	PNIV4	PNIV3	PNIV2	PNIV1	PNIV0
		R	PNO15	PNO14	PNO13	PNO12	PNO11	PNO10	PNO9	PNO8	PNO7	PNO6	PNO5	PNO4	PNO3	PNO2	PNO1	PNO0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
TX / RX FIFO	0x0400 ~0x04F F	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W																
		R																

9.1.1 Reset Register (Address: 0x50001000h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RESETN	FWPRN	FRPRN	FIFORN	BFCRN			
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

RESETN: Soft reset. (Write only)
[1]: Soft reset this device. Auto clear when done.

FWPRN: FIFO write point reset. (Write only)

[1]: reset FIFO write pointer. Auto clear when done.

FRPRN: FIFO read point reset. (Write only)
[1]: reset FIFO read pointer. Auto clear when done.

FIFORN: FIFO data reset. (Write only)
[1]: Reset FIFO Data to all zero. Auto clear when done.

BFCRN: Back-off counter reset. (Write this register to 1 to issue reset command, then it is auto clear.)
[1]: Reset Back-off counter to zero. Auto clear when done.

9.1.2 Strobe Command Register (Address: 0x50001004h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	STRB7	STRB6	STRB5	STRB4	STRB3	STRB2	STRB1	STRB0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

Use strobe command control RF state.
Strobe[7:4] = 4'b1000: Sleep mode.
Strobe[7:4] = 4'b1001: Idle mode.
Strobe[7:4] = 4'b1010: Standby .
Strobe[7:4] = 4'b1011: PLL mode.
Strobe[7:4] = 4'b1100: RX mode
Strobe[7:4] = 4'b1101: TX mode

9.1.3 Mode Control Register (Address: 0x50001008h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	FIFOSS		AIF	DFCD	DFCRC	FMT	FMS	
R	FIFOSS		AIF	CD		FMT	FMS	
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								LENS
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

FIFOSS: FIFO sequence order select.
[0]: LSB first.
[1]: MSB first.

AIF: Auto IF. Recommend AIF = [1].
[0]: Disable.
[1]: Enable.
RF LO frequency will auto offset one IF frequency whenever entering to RX mode.

DFCD (Data Filter by CD): The received packet will be filtered out.
[0]: Disable.
[1]: Enable.

CD: Carrier detector (Read only).

[0]: Input power below threshold.
[1]: Input power above threshold.

DFCRC: Filter RX packet with CRC check.
[0]: Disable.
[1]: Enable.

FMT: Reserved for internal usage only.

FMS: Direct/FIFO mode select.
[0]: Direct mode.
[1]: FIFO mode.

LENS: Length sequence order select.
[0]: LSB first.
[1]: MSB first.

9.1.4 Status Register (Address: 0x50001010h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								
R	CER	XER	PLLER	TRSR	TRER	RFSTATE2	RFSTATE1	RFSTATE0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R	FPEN			CSMAF	CCAF	FPF	FECF	CRCF
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

CER: Chip Status. (Read only)
[0]: Chip is disabled.
[1]: Chip is enabled.

XER: Xtal Status. (Read only)
[0]: Crystal oscillator is disabled.
[1]: Crystal oscillator is enabled.

PLLE: PLL Status. (Read only)
[0]: PLL is disabled.
[1]: PLL is enabled after PLL strobe command.

TRER: TRX Status I. (Read only)
[0]: TRX is disabled.
[1]: TRX is enabled.

TRSR: TRX Status II. (Read only)
[0]: RX mode.
[1]: TX mode.
Serviceable when TRER=1 (TRX is enable).

RFSTATE[2:0]: RF state flag.
RFSTATE[2:0] = 3'b000: Sleep mode.
RFSTATE[2:0] = 3'b001: Idle mode.
RFSTATE[2:0] = 3'b010: standby mode.
RFSTATE[2:0] = 3'b011: PLL mode.
RFSTATE[2:0] = 3'b100: TX mode
RFSTATE[2:0] = 3'b101: RX mode

FPEN: Frame pending bit.

CSMAF: CSMA function flag.
[0]: CSMA pass.

[1]: CSMA Fail.

CCAF: CCA flag.
[0]: CCA pass.
[1]: CCA fail.

FPF: FIFO pointer flag

FECF: FEC flag. (Read only and updated for each valid packet.)
[0]: FEC pass.
[1]: FEC error.

CRCF: CRC flag. (Read only and updated for each valid packet.)
[0]: CRC pass.
[1]: CRC error.

9.1.5 RF interrupt Register (Address: 0x50001014h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	ISTRN						TWIS	FPFIS
R	INT	INTF			IST3	IST2	IST1	IST0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

ISTRN: Interrupt state reset. (write only). Recommend ISTRN = [0].
[1]: Reset interrupts sources. Auto clear when done.

TWIS : TX wake-up interrupt select.
[0]: Before Final TX.
[1]: After Final TX.

INT: Interrupt source state.
[0]: None.
[1]: Busy.
INTF: Interrupt flag.
INTF status is shown as the respective function as the below table.

IST[3:0]: Interrupt source select.

IST[3:0]	Interrupt source	INTF (Bit 0)	Note
0000	none	none	
0001	WTR	CRCF	
0010	CSMA_CA	CSMAF	
0011	CCA	CCAF	
0100	ART	Reserved	
0101	EDM	None	
0110	FPFINT	FPF	
0111	ADCM	None	
1000	WOR	CRCF	
1001	TWOR	None	
1010	WOT	None	

9.1.6 ID I Register (Address: 0x50001014h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
R	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16
R	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24
R	ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24

9.1.7 ID II Register (Address: 0x50001018h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	ID39	ID38	ID37	ID36	ID35	ID34	ID33	ID32
R	ID39	ID38	ID37	ID36	ID35	ID34	ID33	ID32
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40
R	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	ID55	ID54	ID53	ID52	ID51	ID50	ID49	ID48
R	ID55	ID54	ID53	ID52	ID51	ID50	ID49	ID48
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	ID63	ID62	ID61	ID60	ID59	ID58	ID57	ID56
R	ID63	ID62	ID61	ID60	ID59	ID58	ID57	ID56

ID: Serial Packet ID (SID).

9.1.8 FIFO Control Register (Address: 0x50001020h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PHR7	PHR6	PHR5	PHR4	PHR3	PHR2	PHR1	PHR0
R	PHR7	PHR6	PHR5	PHR4	PHR3	PHR2	PHR1	PHR0
R/W								
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	FPM1	FPM0						
R	FPM1	FPM0						

PHR [7:0] : Physical Header of IEEE 802.15.4.
It contains length of frame.
Write : TX FIFO Length.
Read : RX FIFO received length.
Payload length is programmable by PHR [7:0]. The physical FIFO depth is 64 bytes. A8137M0 also supports logical FIFO extension up to 256 bytes.

FPM [1:0]: FIFO Pointer Margin
TX: 8, 12, 16, 32 byte; RX: 56, 52, 48, 32 byte

9.1.9 Data Rate Register (Address: 0x50001024h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
R	SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**

W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

SDR [7:0]: Data Rate Setting. On-air Data rate = MDR / (SDR+1).

9.1.10 RF GIO Register (Address: 0x50001028h)

R/W	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
W		GIO1I			GIO1S3	GIO1S2	GIO1S1	GIO1S0
R						P_IRQ2O	P_IRQ1O	P_CKO
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W		GIO2I			GIO2S3	GIO2S2	GIO2S1	GIO2S0
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W		CKOI				CKOS2	CKOS1	CKOS0
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

GIO1S [3:0]: GIO1 pin function select.

GIO1S	TX state	RX state
[0000]	INT (Interrupt)	
[0001]	WTR (Wait until TX or RX finished)	
[0010]	WOR	
[0011]	EOAC (end of access code)	FSYNC (frame sync)
[0100]	TMEO (TX modulation enable)	CD (carrier detect)
[0101]	Preamble Detect Output (PMDO)	
[0110]	RXD (Direct mode)	
[0111]	TXD (Direct mode)	
[1000]	PDN_RX	
[1001]	PDN_TX	
[1010]	PASW	
[1011]	VTB[0]	
[1100]	DMII	
[1101]	EOFF	
[1110]	FPF	
[1111]	CKE	

GIO1I: GIO1 pin output signal invert.
[0]: Non-inverted output.
[1]: Inverted output.

GIO2S [2:0]: GIO2 pin function select.

GIO2S	TX state	RX state
[0000]	INT	
[0001]	WTR (Wait until TX or RX finished)	
[0010]	Wake up signal	
[0011]	EOAC (end of access code)	FSYNC (frame sync)
[0100]	TMEO (TX modulation enable)	CD (carrier detect)
[0101]	Preamble Detect Output (PMDO)	
[0110]	RXD (Direct mode)	
[0111]	TXD (Direct mode)	
[1000]	PDN_RX	

[1001]	PDN_TX
[1010]	PASW
[1011]	VTB[1]
[1100]	DMIQ
[1101]	EOFF
[1110]	FPF
[1111]	CKE

EOFF: EOP, EOVBC, EOFBC, EOADC, EOVCC, EOVDC, EORSSC, OKADC, EOAGC (Internal usage only).

GIO2I: GIO2 pin output invert.
[0]: Non-inverted output.
[1]: Inverted output.

CKOS [2:0]: CKO pin output select.
[000]: INTF (refer to 30h).
[001]: BDF (Low battery detection output).
[010]: XRDY.
[011]: SDO (4 wires SPI data output).
[100]: BBCK (4XDR).
[101]: RO 320us. (20 symbols).
[110]: RO frequency.
[111]: Data clock (2M or 250K).

CKOI: CKO pin output signal invert.
[0]: Non-inverted output.
[1]: Inverted output.

9.1.11 Calibration Control Register (Address: 0x50001080h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W				RSSC	VDC	VCC	VBC	FBC
R				RSSC	VDC	VCC	VBC	FBC
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

RSSC: RSSI calibration (Auto clear when done).
[0]: Disable.
[1]: Enable.

VDC: VCO deviation calibration (Auto clear when done).
[0]: Disable.
[1]: Enable.

VCC: VCO current calibration (Auto clear when done).
[0]: Disable.
[1]: Enable.

VBC: VCO bank calibration (Auto clear when done).
[0]: Disable.
[1]: Enable.

FBC: IF filter bank Calibration (Auto clear when done).
[0]: Disable.
[1]: Enable.

9.1.12 IF Control Register (Address: 0x50001084h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W			IFAS	MFBS	MFB3	MFB2	MFB1	MFB0
R			IFAS	FBCF	FB3	FB2	FB1	FB0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R				FCD4	FCD3	FCD2	FCD1	FCD0
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

IFAS: IF amplifier current setting. Recommend IFAS = [0].

MFBS: IF filter calibration select. Recommend MFBS = [0].
[0]: Auto.
[1]: Manual.

MFB [3:0]: IF filter manual calibration value.

FBCF: IF filter calibration flag.
[0]: Pass.
[1]: Fail.

FB [3:0]: IF filter calibration result (read only).
Auto calibration result when MFBS = 0.
Manual calibration result when MFBS = 1.

FCD [4:0]: IF filter calibration difference.

9.1.13 VCO Current Register (Address: 0x50001088h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PKTH	PKS	VCCS	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
R				FVCC	VCB3	VCB2	VCB1	VCB0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W							PKT1	PKT0
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

PKTH: VCO Peak Detect threshold Select. Recommend PKIS = [00].

PKS: VCO Current Calibration Mode Select. Recommend PKS = [1].

VCCS: VCO current calibration value select.

MVCS: VCO current calibration select. Recommend MVCS = [0].
[0]: Auto.
[1]: Manual.

VCOC [3:0]: VCO current manual calibration value.
VCO current manual setting when MVCS = 1.

FVCC: VCO current calibration flag.
[0]: Pass.
[1]: Fail.

VCB [3:0]: VCO current calibration value (read only).
Auto calibration result when MVCS = 0.
Manual calibration result when MVCS = 1.

PKT[1:0]: VCO Peak Detect Current Select. Recommend PKT = [00].

9.1.14 VCO band Register (Address: 0x5000108Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W				MVBS	MVB3	MVB2	MVB1	MVB0
R				VBCF	VB3	VB2	VB1	VB0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	MDAG7	MDAG6	MDAG5	MDAG4	MDAG3	MDAG2	MDAG1	MDAG0
R	ADAG7	ADAG6	ADAG5	ADAG4	ADAG3	ADAG2	ADAG1	ADAG0
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								MDAGS
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

MVBS: VCO bank calibration select. Recommend MVBS = [0].
[0]: Auto.
[1]: Manual.

MVB [2:0]: VCO band manual calibration value.
VCO band manual setting when MVBS = 1.

VBCF: VCO band calibration flag.
[0]: Pass.
[1]: Fail.

VB [2:0]: VCO bank calibration value (read only).
Auto calibration result when MVBS = 0.
Manual calibration result when MVBS = 1.

MDAG [7:0]: DAG manual calibration value. Recommend MDAG = [0x80].

ADAG [7:0]: DAG auto calibration result (read only).

MDAGS: DAG calibration select. Recommend MDAGS = [0].
[0]: Auto.
[1]: Manual.

9.1.15 VCO Deviation I Register (Address: 0x50001090h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
R	VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W							CSW	DEVCM
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

VMG [7:0]: VM Center Value for Deviation Calibration. Recommend VMG [7:0] = [0x80].

CSW: Clock Disable for VCO Modulation. Recommend CSW = [1].
[0]: Enable.
[1]: Disable.

DEVCM: DEV calibration mode.
[0]: signal side mode.
[1]: double side mode.

9.1.16 VCO Deviation II Register (Address: 0x50001094h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	DEVS3	DEVS2	DEVS1	DEVS0	DAMR_M	VMTE_M	VMS_M	MSEL
R	DEVA7	DEVA6	DEVA5	DEVA4	DEVA3	DEVA2	DEVA1	DEVA0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	MVDS	MDEV6	MDEV5	MDEV4	MDEV3	MDEV2	MDEV1	MDEV0
R	ADEV7	ADEV6	ADEV5	ADEV4	ADEV3	ADEV2	ADEV1	ADEV0
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

DEVS [3:0]: Deviation output scaling. Recommend DEVS = [0011].

DAMR_M: DAMR manual enable. Recommend DAMR_M = [0].
[0]: Disable.
[1]: Enable.

VMTE_M: VMT manual enable. Recommend VMTE_M = [0].
[0]: Disable.
[1]: Enable.

VMS_M: VM manual enable. Recommend VMS_M = [0].
[0]: Disable.
[1]: Enable.

MSEL: VCO control select. Recommend MSEL = [0].
[0]: Auto control for VMS /VMTE / DAMR.
[1]: Manual control for VMS /VMTE / DAMR.

DEVA [7:0]: VCO Deviation result.
Auto calibration result when MVDS = 0. (1Fh)
Manual calibration result when MVDS = 1. (1Fh)
Where auto calibration result is ((ADEV / 8) × (DEVS + 1)).

MVDS: VCO deviation calibration select. Recommend MVDS = [0].
[0]: Auto.
[1]: Manual.

MDEV [6:0]: VCO deviation manual calibration value.

ADEV [7:0]: VCO deviation auto calibration value.

9.1.17 Channel Register (Address: 0x500010C0h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
R	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**

W								
R								

CHN [7:0]: RF Channel Number.

9.1.18 Radio Frequency I Register (Address: 0x500010C4h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								BIP8
R								

BIP [8:0]: LO frequency integer part setting.

Xtal	Data Rate	BIP [8:0]
16MHz	2Mbps	0x0096
18MHz	3Mbps	0x005

BFP [15:0]: LO frequency floating part setting.

Xtal	Data Rate	BFP [15:0]
16MHz	2Mbps	0x0004
18MHz	3Mbps	0x5558

9.1.19 Radio Frequency II Register (Address: 0x500010C8h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CHR7	CHR6	CHR5	CHR4	CHR3	CHR2	CHR1	CHR0
R	CHR7	CHR6	CHR5	CHR4	CHR3	CHR2	CHR1	CHR0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W		CHR14	CHR13	CHR12	CHR11	CHR10	CHR9	CHR8
R		CHR14	CHR13	CHR12	CHR11	CHR10	CHR9	CHR8
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	CHI3	CHI2	CHI1	CHI0	CHD3	CHD2	CHD1	CHD0
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

CHR [14:0]: Channel resolution setting.

Xtal	Data Rate	CHR [14:0]
16MHz	2Mbps	0x000
18MHz	3Mbps	0x071C

Remark: The above setting is used for 500KHz channel spacing.

CHI [3:0]: Auto IF offset channel number setting.
If F_{CHSP} = 500 KHz, recommend **CHI = [0011]**.
F_{CHSP} × (CHI + 1) = 2MHz.

Xtal	Data Rate	CHI [3:0]
16MHz	2Mbps	0011
18MHz	3Mbps	0101

CHD [3:0]: Channel frequency offset for deviation calibration.
If F_{CHSP} = 500 KHz, recommend **CHD = [0111]**.

Where Offset channel number = +/- (CHD + 1).

Xtal	Data Rate	CHD [3:0]
16MHz	2Mbps	0111
18MHz	3Mbps	1011

9.1.20 Channel Group Register (Address: 0x500010CCh)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
R	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0
R	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

CHGL [7:0]: PLL channel group low boundary setting. Recommend CHGL = [0x3C].

CHGH [7:0]: PLL channel group high boundary setting. Recommend CHGH = [0x78].

9.1.21 TX Control Register (Address: 0x50010100h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PPS	TCPS	DEVSUB	GDR	FS	TXDI	TMDE	TME
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W						FPS2	FPS1	FPS0
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

PPS: TX delay fit data select.
[0]: Fit preamble carrier.
[1]: Fit SID data.

TCPS: TX delay fit carrier or preamble select(turbo mode).
[0]: Fit TX carrier.
[1]: Fit preamble data.

DEVSUB: TX deviation scale.
[0]: 1x.
[1]: 0.9x.

GDR: Gaussian Filter Over-sampling Rate select.
[0]: BT= 1.4~0.6
[1]: BT= 0.7~0.55

FS: Gaussian Filter Select.
[0]: Disable.
[1]: Enable.
Note: Please contact AMICCOM FAE for using Gaussian Filter.

TXDI: TX data invert. Recommend TXDI = [0].
[0]: Non-invert.

[1]: Invert.

TMDE: TX Modulation Enable for VCO Modulation. Recommend TMDE = [1].
[0]: Disable.
[1]: Enable.

TME: TX modulation enable.
[0]: Disable.
[1]: Enable.

FPS[2:0]: GF parameter select.
GDR=0

FPS[2:0]	7	6	5	4	3	2	1	0
BT	1.4	1.3	1.2	1.1	0.75	0.7	0.65	0.6

GDR=1

FPS[2:0]	7	6	5	4	3	2	1	0
BT	0.7	0.65	0.6	0.55	0.7	0.65	0.6	0.55

9.1.22 TX Gain Register (Address: 0x50010104h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PWORS	TXCS	PAC2	PAC1	PAC0	TBG2	TBG1	TBG0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W					PAV1	PAV0	PAB_HCS	PA_HCS
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	IBPAS	VBPAS	PGV_PA1	PGC_PA0	PA_TX1			
R								

PWORS: Reserved for internal usage only.

TXCS: TX current select.

PAC [2:0]: PA Current Setting.

TBG [2:0]: TX Buffer Setting.

PAV[1:0]: PA voltage. Reserved for internal usage only.

PA_HCS, PAB_HCS: Reserved for internal usage only.

IBPAS,VBPAS,PGV_AP[1:0],PA_TX1: PA power control. Reserved for internal usage only.

9.1.23 TX Power Register (Address: 0x50010108h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W				TXUDS1	TXUDS0	TRT2	TRT1	TRT0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W						RAMP2	RAMP1	RAMP0
R								

TXUDS [1:0]: TX ramp up/down clock select.
[00]: 4M
[01]: 2M
[10]: 1M
[11]: 0.5M.

TRT [2:0]: Reserved for internal usage only.

RAMP [2:0]: TX switch signal select. Reserved for internal usage only.

9.1.24 TX Modulation Register (Address: 0x5001010Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W						FDP2	FDP1	FDP0
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	DEVFD1	DEVFD0	DEVD2	DEVD1	DEVD0	DEVGD2	DEVGD1	DEVGD0
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	XDS				DEVDS	DAMV1	DAMV0	DEVFD2
R								

FD [7:0]: Frequency deviation setting. Recommend FD = [0x40]
Frequency deviation:
$_{DEV}= F_{PFD}$ x 127 x (FD [7:0] + 1) x $2^{(FDP\ [2:0]\ +\ 1)}$ / 2^{25}

FDP [2:0]: Frequency deviation power setting. Recommend FDP = [111].

DEVFD [2:0]: Reserved for internal usage only.

Xtal	Date Rate	DEVFD [2:0]
16MHz	2Mbps	000
18MHz	3Mbps	000

DEVD [2:0]: Reserved for internal usage only.

Xtal	Data Rate	DEVD [2:0]
16MHz	2Mbps	011
18MHz	3Mbps	011

Recommend F_{DEV} = 500 KHz.

DEVGD [2:0]: Sigma Delta Modulator Data Delay Setting. Recommend DEVGD = [000].

XDS: VCO Modulation Data Sampling Clock selection. Recommend XDS = [1].
[0]: 8x over-sampling Clock.
[1]: XCPCK Clock.

DAMV [1:0]: Demodulator D/A Voltage Range Select. Recommend DAMV = [11].
[00]: 1/32*1.2.
[01]: 1/16*1.2.
[10]: 1/8*1.2.
[11]: 1/4*1.2.

9.1.25 RX Control Register (Address: 0x50010140h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W						RXDI	DMG	ULS
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								

R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

RXDI: RX data output invert. Recommend RXDI = [0].
[0]: Non-inverted output.
[1]: Inverted output.

DMG: Reserved for internal usage only.

ULS: RX Up/Low side band select. Recommend ULS = [0].
[0]: Up side band.
[1]: Low side band.

9.1.26 RX Gain I Register (Address: 0x50010144h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W			IGS1	IGS0	MGS1	MGS0	LGS1	LGS0
R			IGS1	IGS0	MGS1	MGS0	LGS1	LGS0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R							VTB1	VTB0
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	PKIS1	PKIS0	VTHS2	VTHS1	VTHS0	VTLS2	VTLS1	VTLS0
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								IFPK
R								

IGS [1:0]: IF gain select. Recommend IGS = [11].
[00]: 0dB.
[01]: 6dB.
[10]: 12dB.
[11]: 18dB.

MGS [1:0]: Mixer gain attenuation select. Recommend MGS = [11].
[00]: 0dB.
[01]: 6dB.
[10]: 12dB.
[11]: 18dB.

LGS [1:0]: LNA gain attenuation select. Recommend LGS = [11].
[00]: 0dB.
[01]: 6dB.
[10]: 12dB.
[11]: 18dB.

VTB: AGC status from Peak detect

PKIS[1:0]: AGC Peak Detect Current Select. Recommend PKIS = [00].

VTHS: AGC target upper limit. Recommand value= [001].

VTLS: AGC target lower limit. Recommand value= [001].

IFPK: AGC Amplifier Current Select. Recommend IFPK = [0].

9.1.27 RX Gain II Register (Address: 0x50010148h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

W				AGCS1	AGCS0	AGCKS1	AGCKS0	AGCE
R								AGCE
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W		MHC3	MHC2	MHC1	MHC0	LHC2	LHC1	LHC0
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

AGCS [1:0]: AGC stop mode. Recommend AGCS = [00].
[00]: Stop by PRAOK.
[01]: Stop by FSYNC.
[10]: Non-stop.
[11]: AGC test mode.

AGCKS [1:0]: AGC clock seleck.
[00]: 4XMDR
[01]: 2XMDR
[10]: 1XMDR
[11]: 1/2XMDR

AGCE: AGC enable. Recommend AGCE = [1].
[0]: Disable.
[1]: Enable.

MHC[3:0]: Mixer Current Control.

LHC[2:0]: LNA Current Control.

9.1.28 RX DEM I Register (Address: 0x50010150h)

R/W	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
W		DCKS	RCP2	RCP1	RCP0	SLF2	SLF1	SLF0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

DCKS: RX data clock select.
[0]: Virtual clock.
[1]: Recovery clock.

RCP [2:0]: Turbo mode recovery clock position. Recommend RCP = [010].

SLF [2:0]: Reserved for internal usage only.

9.1.29 RX DEM II Register (Address: 0x50010154h)

R/W	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
W	DCV7	DCV7	DCV7	DCV7	DCV7	DCV7	DCV7	DCV7
R	DCO7	DCO6	DCO5	DCO4	DCO3	DCO2	DCO1	DCO0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W							DCM1	DCM0

R							DCM1	DCM0
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

DCV [7:0]: Demodulator fix mode DC value. Recommend DCV = [0x80].

DCO[7:0]: DC average output (read only).

DCM[1:0] : Demodulator DC estimation mode. Recommend DCM = [01].
[00]: Fix mode (For ±10 ppm crystal accuracy only). DC level is set by DCV [7:0].
[01]: 32 bits average before frame sync, hold after frame sync.
[1X]: 32 bits average before frame sync and then become 128 bits average after frame sync.

9.1.30 CODE I Register (Address: 0x50010180h)

R/W	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
W					CRCIV	WHTS	FECS	CRCS
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W		ETH2	ETH1	ETH0	PTH2	PTH1	PTH0	IDL
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

CRCIV: CRC format invert.
[0]:normal
[1]:invert.

WHTS: Data whitening (Data Encryption) select.
[0]: Disable.
[1]: Enable.

FECS: FEC select.
[0]: Disable.
[1]: Enable.

CRCS: CRC select.
[0]: Disable.
[1]: Enable.

ETH [2:0]: Received SID2 Code Error Tolerance. SID2 is only valid if ID length is 8bytes.
[000]: 0 bit,
[001]: 1 bit.
[010]: 2 bit.
[011]: 3 bit.
[100]: 4 bit,
[101]: 5 bit.
[110]: 6 bit.
[111]: 7 bit.

PTH [2:0]: Received SID1 Code Error Tolerance.
[000]: 0 bit,
[001]: 1 bit.
[010]: 2 bit.
[011]: 3 bit.

[100]: 4 bit,
[101]: 5 bit.
[110]: 6 bit.
[111]: 7 bit.

IDL: ID code length select.
[0]: 4 bytes.
[1]: 8 bytes.

9.1.31 CODE II Register (Address: 0x50010184h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W		WS6	WS5	WS4	WS3	WS2	WS1	WS0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

WS [6:0]: Data Whitening seed setting (data encryption key).

9.1.32 CODE III Register (Address: 0x50010188h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CRCPL7	CRCPL6	CRCPL5	CRCPL4	CRCPL3	CRCPL2	CRCPL1	CRCPL0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	CRCPL15	CRCPL14	CRCPL13	CRCPL12	CRCPL11	CRCPL10	CRCPL9	CRCPL8
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

CRCPL[15:0]: CRC polynorminal value.

9.1.33 CODE IV Register (Address: 0x5001018Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CRCRIV7	CRCRIV6	CRCRIV5	CRCRIV4	CRCRIV3	CRCRIV2	CRCRIV1	CRCRIV0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	CRCRIV15	CRCRIV14	CRCRIV13	CRCRIV12	CRCRIV11	CRCRIV10	CRCRIV9	CRCRIV8
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	CRCTIV7	CRCTIV6	CRCTIV5	CRCTIV4	CRCTIV3	CRCTIV2	CRCTIV1	CRCTIV0
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	CRCTIV15	CRCTIV14	CRCTIV13	CRCTIV12	CRCTIV11	CRCTIV10	CRCTIV9	CRCTIV8
R								

CRCRIV[15:0]: CRC RX initial value.

CRCTIV[15:0]: CRC TX initial value.

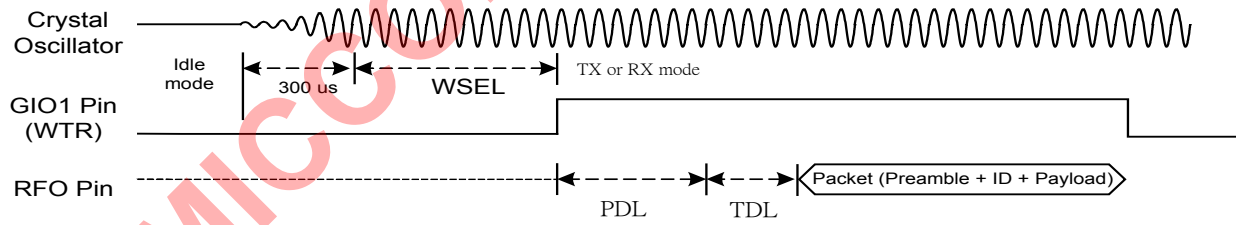
9.1.34 DELAY Register (Address: 0x500101C0h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PADL		TDL2	TDL1	TDL0		PDL1	PDL0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	WSEL2	WSEL1	WSEL0	AGC_D1	AGC_D0		RS_DLY1	RS_DLY0
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W					PTRS3	PTRS2	PTRS1	PTRS0
R								

PADL: Embedded PA off delay.
[0]: 8us.
[1]: 0us.

TDL [2:0]: TRX Settling Delay. Recommend TDL = [100].
[000]: 0us.
[001]: 16us.
[010]: 32us.
[011]: 48us.
[100]: 64us.
[101]: 80us.
[110]: 96us.
[111]: 112us.

PDL [1:0]: PLL Settling Delay. Recommend PDL = [10].
[00]: 0us.
[01]: 16us.
[10]: 32us.
[11]: 48us.



WSEL [2:0]: XTAL settling delay (0us ~ 2000us). Recommend WSEL = [011].
[000]: 0us.
[001]: 200us.
[010]: 400us.
[011]: 600us.
[100]: 800us.
[101]: 1000us.
[110]: 1500us.
[111]: 2000us.

AGC_DLY [1:0]: AGC Settling Delay (4us ~ 16us). Recommend AGC_DLY = [00].
[00]: 4us.
[01]: 8us.
[10]: 12us.
[11]: 16us.

RS_DLY [1:0]: AGC Measurement Delay . Recommend RS_DLY = [01].
[00]: 2XAGCK count.
[01]: 3XAGCK count.
[10]: 4XAGCK count.
[11]: 5XAGCK count.

PTRS [3:0]: Pre_TRX setting. Recommend PTRS = [0000].

9.1.35 RF CK Control I Register (Address: 0x500101C4h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CGFS1	CGFS0	MDR1	MDR0	GRC3	GRC2	GRC1	GRC0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								HFR
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	CGC1	CGC0	CGS		XCP	XCC	XS	XEC
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								RDU
R								

CGFS [1:0]: Clock generator frequency select. Recommed CGFS = [01].
[00]: 16MHz.
[01]: 32MHz.
[10]: 48MHz.
[11]: 64MHz.

MDR [1:0]: Main Data rate setting.

MDR [1:0]	Data Rate
[00]	Reserved
[01]	1 Mbps
[10]	2 Mbps
[11]	Reserved

GRC [3:0]: Generator Reference Counter
GRC is used to get internal 2 MHz Clock Generator Reference (F_{CGR}) for different Xtal frequency.

External Crystal (F_{XREF})	Clock Generation Reference (CGR)	GRC [3:0]
16 MHz	Must be 2 MHz	[0111]
12 MHz	Must be 2 MHz	[0101]
8 MHz	Must be 2 MHz	[0011]

HFR: Helf frequency rate select. Recommend HFR = [1].
[0]: 32x.
[1]: 16x.

CGC[1:0]: Clock generation current setting.

CGS: Clock generator enable.
[0]: Disable.
[1]: Enable.

XCP: Crystal Oscillator Regulated Couple Setting. Recommend XCP = [1].
[0]: 1.5mA.
[1]: 0.5mA.

XCC : Crystal Startup Current Selection. Recommend XCC = [1].
[0]: about 0.7 mA.
[1]: about 1.5 mA.

XS: Crystal oscillator select. Recommend XS = [1].
[0]: Use external clock.

[1]: Use external crystal.

XEC: Crystal enable control.
[0]: Control by RF state.
[1]: Control by MCU and RF state.

RDU: Manual CGC select.(CGS=1) Recommend RDU = [1].

9.1.36 RF CK Control II Register (Address: 0x500101C8h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W			PRIC1	PRIC0	PRRC1	PRRC0	SDPW	NSDO
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

PRRC [1:0]: Reserved for internal usage only.

PRIC [1:0]: Reserved for internal usage only.

9.1.37 Charge Pump Register (Address: 0x500101D0h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CPM3	CPM2	CPM1	CPM0	CPT3	CPT2	CPT1	CPT0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W							CPCH1	CPCH0
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								CPS
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

CPM [3:0]: Charge pump current setting for VM loop. Recommend CPM = [1111].
Charge pump current = (CPM + 1) / 16 mA.

CPT [3:0]: Charge pump current setting for VT loop. Recommend CPT = [0011].
Charge pump current = (CPT + 1) / 16 mA.

CPCH [1:0]: Charge pump high current.

CPS: Reserved for internal usage only.

9.1.38 RF TEST I Register (Address: 0x500101D4h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W			CSXTL5	CSXTL4	CSXTL3	CSXTL2	CSXTL1	CSXTL0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								

R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

CSXTL[5:0]: On-chip capacitor added on XI, XO pin, respectively.

CSXTL is the on-chip capacitor for XTAL oscillator to fine tune offset frequency of the wanted RF carrier.
The capacitance= (CSXTL [4:0] + CSXTL [5]*16) pF.

9.1.39 RF TEST II Register (Address: 0x500101D8h)

R/W	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
W			STM5	STM4	STM3	STM2	STM1	STM0
R			STMR5	STMR4	STMR3	STMR2	STMR1	STMR0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W			BDC5	BDC4	BDC3	BDC2	BDC1	BDC0
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	FGC1	FGC0	CTR5	CTR4	CTR3	CTR2	CTR1	CTR0
R	FGCR1	FGCR0	CTRR5	CTRR4	CTRR3	CTRR2	CTRR1	CTRR0
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

STM: Reserved for internal usage.
BDC[3:0]: Battery detector current option select.
FGC, CTR, Reserved for internal usage.
Recommend FGC = [10].

9.1.40 TEST III Register (Address: 0x500101DCh)

R/W	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
W	VTRB3	VTRB2	VTRB1	VTRB0	VMRB3	VMRB2	VMRB1	VMRB0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W						INTPRC	VRPL1	VRPL0
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

VTRB [3:0]: Resistor Bank for VT RC Filtering.

VMRB [3:0]: Resistor Bank for VM RC Filtering.

INTPRC: Internal PLL loop filter resistor and capacitor select. Recommend INTPRC = [1].
[0]: disable. **[1]:** enable

VRPL [1:0]: internal PLL loop filter resistor value select. Recommend VRPL = [00].
[00]: 500 ohm. **[01]:** 666 ohm. **[10]:** 1 K ohm. **[11]:** 2K ohm.

9.1.41 IF TEST I Register (Address: 0x500101E0h)

R/W	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
W	TXLO_HC	RXLO_HC	VCBS1	VCBS0	IFBC1	IFBC0	LIMC	IFAS
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	PRS	QLIM	LOVRS	LNAVRS	TLB1	TLB0	RLB1	RLB0

R								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								

TXLO_HC: TX LO high current.
RXLO_HC: RX LO high current.

VCBS [1:0]: VCO Buffer current Select. Recommend VCBS = [10].
[00]: 0.6mA. **[01]:** 0.8mA. **[10]:** 1.0mA. **[11]:** 1.2mA.

IFBC [1:0]: IF BPF current Select. Recommend IFBC = [10].

LIMC: IF limiter current select. Recommend LIMC = [1].
[0]: 0.3mA. **[1]:** 0.6mA.

IFAS: IF amplifier current setting. Recommend IFAS = [0].

PRS: Reserved for internal usage only.

QLIM: quick charge select for IF limiter amp. Recommend QLIM=1.

[0]: enable. [1]: disable.

LOVRS: LO voltage reference select.

LNAVRS: LNA voltage reference select.

TLB [2:0]: RF TX LO Buffer Current Select.
[00]: TBD. **[01]:** TBD. **[10]:** TBD.. **[11]:** TBD.

RLB [2:0]: RF RX LO Buffer Current Select.
TBD

9.1.42 IF TEST II Register (Address: 0x500101E4h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								TRDC
R								
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W			IFFATS	IFTS	ATP3	ATP2	ATP1	ATP0
R								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								

TRDC: RFIO pin and RFO pin control.
[0]: Internal Combined.
RFIO pin is Input/Output (bi-directional for PA output and LNA input).
RFO pin is NC.

[1]: External Combined.
RFIO pin is Input (single-directional for LNA input).
RFO pin is Output (single-directional for PA output).

IFFATS: Reserved for internal usage only.

IFTS: Reserved for internal usage only.

ATP [3:0]: RF Analog test Pin Configuration. Recommend ATP = [0000].

{IFTS, ATP [3], ATP [1:0]}	VDD_R
[XX00]	1.8V Reference voltage
[XX01]	Analog temperature voltage
[0X10]	IF filter positive output
[0X11]	IF filter negative output
[1010]	IF amplifier positive output
[1011]	IF amplifier negative output
[1110]	Mixer positive output
[1111]	Mixer negative output

9.1.43 WOR/WOT I Register (Address: 0x50010200h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W						WORE	WOTE	TWWS
R						WORE	WOTE	
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W			WUS1	WUS0	WTLP3	WTLP2	WTLP1	WTLP0
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								RNTWUNF
R								TWUNF
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

WORE: Wake On RX enable.
[0]: Disable. **[1]:** Enable.

WOTE: Wake On TX enable.
[0]: Disable. **[1]:** Enable.

TWWS: Wake On Timer enable.
[0]: Disable. **[1]:** Enable.

WUS [1:0]: Wake up select when WOR is enabled.
[00]: Detect carrier.
[01]: Detect IEEE 802.15.4 Sync word.
[10]: Detect IEEE 802.14.4 Beacon.
[11]: CRC pass.

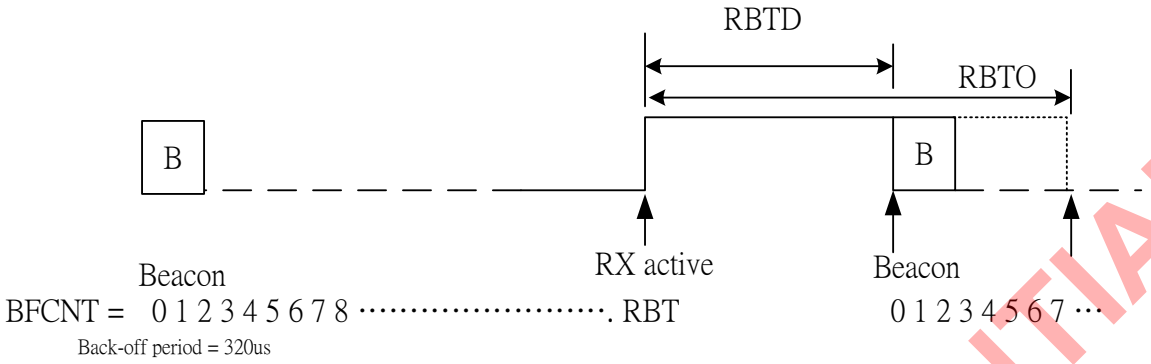
WTLP[3:0]: WOT loop time.
RNTWUNF: Reset TWUN flag.
TWUNF: TWUN flag.

9.1.44 WOR/WOT II Register (Address: 0x50010204h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RBTO7	RBTO6	RBTO5	RBTO4	RBTO3	RBTO2	RBTO1	RBTO0
R	RBTD7	RBTD6	RBTD5	RBTD4	RBTD3	RBTD2	RBTD1	RBTD0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	RBTO15	RBTO14	RBTO13	RBTO12	RBTO11	RBTO10	RBTO9	RBTO8
R	RBTD15	RBTD14	RBTD13	RBTD12	RBTD11	RBTD10	RBTD9	RBTD8
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

RBTO [15:0]: Random back off time-out in RX.
Time-out = (RBTO+1) X 320 us.

RBTD [15:0]: Random back off difference.
The difference is the value between the active position and the beacon position.



9.1.45 WOR/WOT III Register (Address: 0x50010208h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RBT7	RBT6	RBT5	RBT4	RBT3	RBT2	RBT1	RBT0
R	BFCNT7	BFCNT6	BFCNT5	BFCNT4	BFCNT3	BFCNT2	BFCNT1	BFCNT0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	RBT15	RBT14	RBT13	RBT12	RBT11	RBT10	RBT9	RBT8
R	BFCNT15	BFCNT14	BFCNT13	BFCNT12	BFCNT11	BFCNT10	BFCNT9	BFCNT8
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	RBT23	RBT22	RBT21	RBT20	RBT19	RBT18	RBT17	RBT16
R	BFCNT23	BFCNT22	BFCNT21	BFCNT20	BFCNT19	BFCNT18	BFCNT17	BFCNT16
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

RBT [23:0]: Random back off active position. (write only)
Active time = (**RBT**+1) X 320us.

BFCNT [23:0]: Random back off counter. (read only)
It could show the position after enable back-off counter or received the beacon frame.
Each back off period is **320us**.
Use the **BFCNT** to calculate the active position (**RBT**).

9.1.46 8BIT ADC Control Register (Address: 0x50010240h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	ADCC	ADCOM1	ADCOM0	AVGS1	AVGS0	ARSSI	CDM	ADCM
R	ADCC	ADCOM1	ADCOM0	AVGS1	AVGS0	ARSSI	CDM	ADCM
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

ADCC: ADC calibration (Auto clear when done).
[0]: Disable. **[1]:** Enable.

ADCOM: ADC output mode. Recommend ADCOM = [10].
[00]: Single mode.
[01]: Average mode (2, 4, 8, 16 average is according to AVGS [1:0].
[10]: ED. No hold.

[11]: ED. Hold after sync 128us.

AVGS [1:0]: ADC average mode. Recommend AVGS = [11].
[00]: 2. **[01]:** 4. **[10]:** 8. **[11]:** 16.

ARSSI: Auto RSSI measurement whenever in RX mode. Recommend ARSSI = [1].
[0]: Disable. **[1]:** Enable.

CDM: CD margin = CDTH – CDTL. Recommend CDM = [1].
[0]: 6 LSB. **[1]:** 12 LSB.

ADCM: ADC measurement (Auto clear when done).
[0]: Disable. **[1]:** Enable.

ADCM	Standby mode	RX mode
[0]	Disable ADC	Disable ADC
[1]	Measure temperature or external voltage	Measure RSSI, carrier detect

9.1.47 8Bit ADC Threshold Register (Address: 0x50010244h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CDTH7	CDTH6	CDTH5	CDTH4	CDTH3	CDTH2	CDTH1	CDTH0
R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

CDTH [7:0]: Carrier detect threshold (write only).

ADC [7:0]: ADC digital output value (read only).

ADC input voltage = 1.2 * ADC [7:0] / 256 V.

9.1.48 8Bit ADC CAL Register (Address: 0x50010248h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	MRHL	RSSL6	RSSL5	RSSL4	RSSL3	RSSL2	RSSL1	RSSL0
R	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W			CRS2	CRS1	CRS0	SRS2	SRS1	SRS0
R	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R	ADL7	ADL6	ADL5	ADL4	ADL3	ADL2	ADL1	ADL0
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R	ADH7	ADH6	ADH5	ADH4	ADH3	ADH2	ADH1	ADH0

MRHL: AGC Manual scale select. Recommend MRHL = [0].
[0]: By (RL−RH). **[1]:** By RSSL[6:0].

RSSL[4:0]: AGC Manual Scale setting. Recommend RSSL = [00000].

RL [7:0]: RSSI Calibration Low Threshold (read only).

RH [7:0]: RSSI Calibration High Threshold (read only).

CRS, SRS: RSSI Calibration parameter. Reserved for internal usage.

ADH[7:0]: AD high level calibration result.

ADL[7:0]: AD low level calibration result.

9.1.49 RF4CE Mode Select Register (Address: 0x50010300h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CCAS		LQIS	ACKS	ARTS	CSMAS	SLOT	DLS
R	CCAS							
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	FMSS						ERX	EDS
R								EDS
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W				CCAM1	CCAM0	SLT2	SLT1	SLT0
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

CCAS: CCA function. (Auto clear when done).
[0]: Disable. **[1]:** Enable.

LQIS: LQI Select. Recommend LQIS = [1].
[0]: Disable. **[1]:** Enable.

ACKS: Auto ACK enable.
[0]: Disable. **[1]:** Enable.

ARTS: Auto Resend enable.
[0]: Disable. **[1]:** Enable.

CSMAS: CSMA-CA enable.
[0]: Disable. **[1]:** Enable.

SLOT: CSMA_CA algorithm type.
[0]: Un-slotted. **[1]:** Slotted.

DLS: Dynamic length select.
[0]: deselect. **[1]:** select.

FMSS: FMS select for EDS/CCA.
[0]: Normal FMS.
[1]: For CCA and ED. When CCA or ED active, FMS = 0.

ERX: RX Behavior.
[0]: Normal RX.
[1]: For CCA and ED. When CCA or ED is done, auto back to previous state (i.e. Standby or PLL mode).

EDS: Energy detect. (Auto clear when done).
[0]: Disable. **[1]:** Enable.

CCAM[1:0]: CCA mode. Recommend CCAM = [01].
[00]: CCAF=1, when RSSI > RTH, and detect preamble frame.
[01]: CCAF=1, when RSSI > RTH.
[10]: CCAF=1, when detect preamble frame.
[11]: CCAF=1, when RSSI > RTH or detect preamble frame.

SLT[2:0]: TRX lead time in slotted mode.
[000]: 2 slot time. **[001]:** 3 slot time. **[010]:** 4 slot time. **[011]:** 5 slot time. **[100]:** 6 slot time. **[101]:** 7 slot time.
[110]: 8 slot time. **[111]:** 9 slot time.

9.1.50 RF4CE CSMA-CA Register (Address: 0x50010304h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	MaxBE3	MaxBE2	MaxBE1	MaxBE0	MinBE3	MinBE2	MinBE1	MinBE0

R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W			CST1	CST0		MaxNB2	MaxNB1	MaxNB0
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

MaxBE [3:0]: Maxmum back-off exponent in CSMA-CA algorithm. Recommend MaxBE = [0101].

MinBE [3:0]: Minimum back-off exponent in CSMA-CA algorithm. Recommend MinBE = [0011].

CST[1:0]: Carrier sense time. Recommend CST = [00].
[00]:128us. **[01]:**160us. **[10]:** 192us. **[11]:**224us.

MaxNB [2:0]: Loop times for CSMA-CA algorithm. Recommend MaxNB = [100].

9.1.51 RF4CE ART Register (Address: 0x50010308h)

R/W	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
W	RTRAT7	RTRAT6	RTRAT5	RTRAT4	RTRAT3	RTRAT2	RTRAT1	RTRAT0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	RTRTD3	RTRTD2	RTRTD1	RTRTD0	RTTRD3	RTTRD2	RTTRD1	RTTRD0
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W						ATLP2	ATLP1	ATLP0
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

RTRAT [7:0]: RX Active Period of Auto-resend function.
Delay= 16 * (RTRAT [7:0]) us.

RTRTD[3:0]: Delay from TX to RX of Auto-resend function. Recommend RTRTD = [0000].
Delay= 16 * (RTRTD [3:0]) us.

RTTRD [3:0]: Delay from RX to TX of Auto-resend function. Recommend RTTRD = [1000].
Delay= 16 * (RTTRD [3:0]) us.

ATLP [2:0]: Loop times for auto resend algorithm. Recommend ATLP = [011].

9.1.52 RF4CE ACK Register (Address: 0x5001030Ch)

R/W	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
W	AFCF7	AFCF6	AFCF5	AFCF4	AFCF3	AFCF2	AFCF1	AFCF0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	AFCF15	AFCF14	AFCF13	AFCF12	AFCF11	AFCF10	AFCF9	AFCF8
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W					ACKD3	ACKD2	ACKD1	ACKD0
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

AFCF[15:0]: ACK Frame Control Field.
AFCF [15:0] shall be filled in advance based on IEEE 802.15.4 Frame Control Field when ACKS =1 (02h).

ACKD [3:0]: Auto-ACK Delay. Recommend ACKD = [1000] for 128 us.
Delay= 16 * (ACKD [3:0]) us.

9.1.53 RF4CE LQI Register (Address: 0x50010310h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								LQICE
R	LQIV7	LQIV6	LQIV5	LQIV4	LQIV3	LQIV2	LQIV1	LQIV0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

LQICE: LQI Counter enable for WOR, ATRE, RX timeout.
[0]: Disable. **[1]:** Enable.

LQIV [7:0]: Link quality indication value (read only).
LQIV=0x00, low link quality.
LQIV=0xFF, high link quality.

9.1.54 RF4CE ADFC Register (Address: 0x50010314h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	MAXVER0	RESMUX2	RESMUX1	RESMUX0	MBEN			
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	FADDE	ACBEN	ACDAT	ACACK	ACCMD	ACRES	PCORR	MAXVER1
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

FADDE: MAC Address Filtering.
[0]: Disable. **[1]:** Enable.

ACBEN: Accept Beacon frame type (0)
[0]: Reject. **[1]:** Accept.

ACDAT: Accept Data frame type (1)
[0]: Reject. **[1]:** Accept.

ACACK: Accept Ack frame type (2)
[0]: Reject. **[1]:** Accept.

ACCMD: Accept MAC command frame type (3)
[0]: Reject. **[1]:** Accept.

ACRES: Accept Reserved frame type (4,5,6,7)
[0]: Reject. **[1]:** Accept.

PCORR: PAN Coordinator.
[0]: End device. **[1]:** Coordinator.

MAXVER: Max frame version. Recommend MAXVER = [01].

RESMUX: FCF reserved bit mask. Recommend RESMUX = [000].

MBEN: Manual Beacon.

9.1.55 RF4CE PID Register (Address: 0x50010318h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

PID[15:0]: PAN ID Storage.
PID [15:0]: Store PAN_ID for frame filtering.
Default : 0xFFFF.

9.1.56 RF4CE SADD Register (Address: 0x5001031Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	SADD7	SADD6	SADD5	SADD4	SADD3	SADD2	SADD1	SADD0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	SADD15	SADD14	SADD13	SADD12	SADD11	SADD10	SADD9	SADD8
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

SADD[15:0]: Short Address Storage.
SADD [15:0]: Store Short address for frame filtering.
Default : 0xFFFF.

9.1.57 RF4CE LADD1 Register (Address: 0x50010320h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	LADD39	LADD38	LADD37	LADD36	LADD35	LADD34	LADD33	LADD32
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	LADD47	LADD46	LADD45	LADD44	LADD43	LADD42	LADD41	LADD40
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	LADD55	LADD54	LADD53	LADD52	LADD51	LADD50	LADD49	LADD48
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	LADD63	LADD62	LADD61	LADD60	LADD59	LADD58	LADD57	LADD56
R								

9.1.58 RF4CE LADD2 Register (Address: 0x50010324h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	LADD7	LADD6	LADD5	LADD4	LADD3	LADD2	LADD1	LADD0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	LADD15	LADD14	LADD13	LADD12	LADD11	LADD10	LADD9	LADD8
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	LADD23	LADD22	LADD21	LADD20	LADD19	LADD18	LADD17	LADD16
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	LADD31	LADD30	LADD29	LADD28	LADD27	LADD26	LADD25	LADD24
R								

LADD[63:0]: Long Address Storage.
LADD [63:0]: Store Long address for frame filtering.
Default : 0xFFFF-FFFF-FFFF-FFFF.

9.1.59 RF4CE PNG Register (Address: 0x50010328h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PNIV7	PNIV6	PNIV5	PNIV4	PNIV3	PNIV2	PNIV1	PNIV0
R	PNO7	PNO6	PNO5	PNO4	PNO3	PNO2	PNO1	PNO0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	PNIV15	PNIV14	PNIV13	PNIV12	PNIV11	PNIV10	PNIV9	PNIV8
R	PNO15	PNO14	PNO13	PNO12	PNO11	PNO10	PNO9	PNO8
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W							PNS	PNIVS
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

PNS: Reserved.

PNIVS: PN initial seed select. Recommend PNIVS = [0].
[0]: Use RF calibration value. **[1]:** Manual setting by PNIV (35h).

PNO [15:0]: 16-bits Random number generator output.

PNIV [15:0]: Initial value of 16-bits Random number generator.

9.1.60 TX/RX FIFO Register (Address: 0x50010400h~0x500104FFh)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								
R								

9.1.61 USID Register (Address: 0x5000F000h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								
R	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R	DID23	DID22	DID21	DID20	DID19	DID18	DID17	DID16

R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R	DID31	DID30	DID29	DID28	DID27	DID26	DID25	DID24

DID [31:0]: A813704

9.2 Power control register start at Address[31:0]= 50000000

Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
Battery Detect	0x0000	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W												BLE	BDV2	BDV1	BDV0	BDE
		R													BDV2	BDV1	BDV0	BDF
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
Flash Control	0x0004	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W								AUTO	PDNFL2	QDSFL2	PDNFL1	QDSFL1	PDNFH	QDSFH	PDNFL	QDSFL
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 27	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
Power Control I	0x0008	W	BODS	PM1SWE	STDLY1	STDLY0		PSD2	PSD1	PSD0	PD_LVD					CLR	CLR	CLR
		R														BODF	RESETNF	PORF
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	PW1SW1	PW1SW0	CPPSN	PMPAR	CLKSEL2	CLKSEL1	CLKSEL0	PMM	PDNDS	PMVSD		PM1S-	-QD	REGAE	PM3F	STOP
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
Power Control II	0x000C	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W			STND	STNP	STNA	STNPA		REGCS	REGCL	REGVS	CBG4	CBG3	CBG2	CBG1	CBG0	BGS
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
Power Control III	0x0010	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W																
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
DCDC Control	0x0014	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W																
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
CHR control	0x0020	W									SBS_C			WUE_PCHG	WUE_UV	WUE_SB	WUE_CHG	CHRI_RN
		R									OVPF	OTPF	OCPF	PCHGF	UVF	SBF	CHGF	CHRI_F
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W									EXV_TS	CM_TS	CHG_LC	CHR_ILIMC			CHARVS	CHAREN
		R																
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RC Control	0x0040	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W												IRCHC	RTCS	ROE	MRC	RCC
		R																RCC
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
RC Control I	0x0044	W					RCKS1	RCKS0	MVS1	MVS0	CX4	CX3	CX2	CX1	CX0	RCOT2	RCOT1	RCOT0
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W							MRCT9	MRCT8	MRCT7	MRCT6	MRCT5	MRCT4	MRCT3	MRCT2	MRCT1	MRCT0
		R							RCT9	RCT8	RCT7	RCT6	RCT5	RCT4	RCT3	RCT2	RCT1	RCT0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16

RC Target	0x0048	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W					TGNUM 11	TGNUM10	TGNUM9	TGNUM8	TGNUM7	TGNUM6	TGNUM 5	TGNUM4	TGNUM3	TGNUM2	TGNUM1	TGNUM0
		R					NUMLH1 1	NUMLH10	NUMLH9	NUMLH8	NUMLH7	NUMLH6	NUMLH 5	NUMLH4	NUMLH3	NUMLH2	NUMLH1	NUMLH0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
XRC Control	0x0050	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W											EKICR1	EKICR0	XRCS	ENRC	MXRC	XRCC
		R																XRCC
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
XRC Control I	0x0054	W							MVXS1	MVXS0					CI1	CI0	ICONTROL1	ICONTROL0
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W								MTRIM8	MTRIM7	MTRIM6	MTRIM 5	MTRIM4	MTRIM3	MTRIM2	MTRIM1	MTRIM0
		R								TRIM8	TRIM7	TRIM6	TRIM5	TRIM4	TRIM3	TRIM2	TRIM1	TRIM0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
XRC Target	0x0058	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W						XTGNUM 10	XTGNUM9	XTGNUM8	XTGNUM7	XTGNUM6	TGNUM 5	XTGNUM4	XTGNUM3	XTGNUM2	XTGNUM1	XTGNUM0
		R						NUMLH10	NUMLH9	NUMLH8	NUMLH7	NUMLH6	NUMLH 5	NUMLH4	NUMLH3	NUMLH2	NUMLH1	NUMLH0

9.2.1 Battery detect Register (Address: 0x50000000h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W				BLE	BDV2	BDV1	BDV0	BDE
R					BDV2	BDV1	BDV0	BDF
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

BLE: Battery life extension. Reserved for internal usage.

BDV[2:0]: Battery detection voltage.
[000]: 2.0V. **[001]:** 2.1V. **[010]:** 2.2V. **[011]:** 2.3V. **[100]:** 2.4V. **[101]:** 2.5V. **[110]:** 2.6V. **[111]:** 2.7V.

BDE: Battery detection enable.
[0]: Disable. **[1]:** Enable.

BDF: Battery detection flag.
[0]: Low Battery. **[1]:** High Battery.

9.2.2 Flash Control Register (Address: 0x50000004h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	AUTO	PDNFL2	QDSFL2	PDNFL1	QDSFL1	PDNFH	QDSFH	PDNFL
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**

W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

PDNFH, QDSFH, PDNFL, QDSFL, PDNFL1, QDSFL1, PDNFL2, QDSFL2: Flash/Memory/M0 core power control. Use for PM mode.
AUTO: Auto mode of flash pumping circuit.

9.2.3 Power Control I Register (Address: 0x50000008h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PDNDS	PMVSDS		PM1S-	-QD	REGAE	PM3F	STOP
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	PM1SW1	PM1SW0	CPPSN	PMPAR	CLKSEL2	CLKSEL1	CLKSEL0	PMM
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	PD_LVD					CLR	CLR	CLR
R						BODF	RESETNF	PORF
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	BODS	PM1SWE	STDLY1	STDLY0		PSD2	PSD1	PSD0
R								

PDNDS,PMVSDS:PDND/PMVSD control select.(reset value: PDNDS=0,PMVSDS=1)

		PDNDS=0 ; PDNDS=1 PDND		PMVSDS=0 ; PMVSDS=1 PMVSD	
PSNS=1	Normal	1	1	0	1
PSNS=0	PM1	0	1	1	1
	PM2	0	1	1	1
	PM3	0	0	0	0

PM1S(Power Mode 1 select)
[1]: Enable
[0]: Disable

QD(Quick discharge Enable)
[1]: Enable
[0]: Disable

REGAE(RegA Enable)
[1]: Enable
[0]: Disable

PM3F (Power Mode 3 flag)
[1]: EnablePM3. MCU enter PM3 after STOP mode and VDD_D is off
[0]: Disable PM3

STOP (Stop mode)
[1]: Enable
[0]: Disable

CLKSEL[2:0] (Clock Select), Select clock source when enable clock select.

[000]: Clock source div 64 as MCU clock
[001]: Clock source div 2 as MCU clock
[010]: Clock source div 4 as MCU clock
[011]: Clock source div 8 as MCU clock
[100]: Clock source div 16 as MCU clock
[101]: Clock source div 32 as MCU clock
[110]: Clock source div 64 as MCU clock
[111]: Select RTC as CPU clock when CKSE=0; RTC div 2 as CPU clock when CKSE=1

PMM (Power management mode)
[1]: Enable
[0]: Disable

PD_LVD: LVD circuit power down.
When PD_LVD=0 and REGI voltage less than 1.8v, the LVD circuit will generate a low voltage reset signal.
[0]: Power on. [1]: Power down.
PORF (power-on reset flag)
= 1: Occurred Power-on Reset
= 0: No Power-on Reset
RESETNF (resetn flag)
= 1: Occurred ResetN reset
= 0: No ResetN resetno resetn reset
BODF (Low voltage detect) flag
= 1: Occurred Low Voltage Reset
= 0: No Low Voltage reset
CLR (Clear flag)
=1: clear flag.
=0: no clear.

PM1SWE,PM1SW[1:0],CPPSN,PMPAR.(for PM mode control)
STDLY[1:0]: Soft start delay.
BODS: BOD flag select

9.2.4 Power Control II Register (Address: 0x5000000Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	REGCL	REGVS	CBG4	CBG3	CBG2	CBG1	CBG0	BGS
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W			STND	STNP	STNA	STNPA		REGCS
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

REGCL: Low current regulator. Reserved for internal usage.
REGVS: Regulator voltage select. Reserved for internal usage.
CBG [4:0]: Vref calibration.

BGS: Bangap (BG) select:
[0]: Low current BG. [1]: High current BG.
STND,STNP,STNA,STNPA: Soft start for regulator D/P/A.PA
REGCS: Regulator current select. Reserved for internal usage.

9.2.5 Charger Control Register (Address: 0x50000020h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	EXV_TS	CM_TS	CHG_LC	CHR_ILIMC			CHARVS	CHAREN
R								

R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	SBS_C			WUE_PCHG	WUE_UV	WUE_SB	WUE_CHG	CHRI_RN
R	OVPF	OTPF	OCPF	PCHGF	UVF	SBF	CHGF	CHRI_F
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

EXV_TS, CM_TS, CHG_LC, CHR_ILIMC, CHARVS, CHAREN: Charger control setting. Reserved for internal usage.

SBS_C: Set charger in to standby mode. (Reset value = 0).
WUE_X: WU enable for charger interrupt source.
CHRI_RN: Clear charger's interrupt flag CHRI_F.

CHRI_F: Charger interrupt indicator.
PCHGF, UVF, SBF, CHGF: Charger state flag.
OVPF, OTPF, OCPF: Protection flag.

9.2.6 RC Control I Register (Address: 0x50000040h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W				IRCHC	RTCS	ROE	MRC	RCC
R								RCC
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

IRCHC: RC oscillator high current mode select.

RTCS: Sleep timer select.
[0]: RC oscillator (Internal). **[1]:** RTC crystal oscillator (External).

ROE: Enable Internal RC oscillator.
[0]: Disable. **[1]:** Enable.

MRC: RO bank manual calibration.
[0]: Disable. **[1]:** Enable.

RCC: RO bank calibration (Auto clear when done).
[0]: Disable. **[1]:** Enable.

9.2.7 RC Control II Register (Address: 0x50000044h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	MRCT7	MRCT6	MRCT5	MRCT4	MRCT3	MRCT2	MRCT1	MRCT0
R	RCT7	RCT6	RCT5	RCT4	RCT3	RCT2	RCT1	RCT0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W							MRCT9	MRCT8
R							RCT9	RCT8
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	CX4	CX3	CX2	CX1	CX0	RCOT2	RCOT1	RCOT0
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W					RCKS1	RCKS0	MVS1	MVS0

R								

MRCT [9:0]: RO Bank manual calibration value (write only).
Manual setting when MRC =1.

RCT [9:0]: RO Bank auto calibration value (read only).

CX[4:0]: Reserved for internal usage only.

RCOT[2:0]: Reserved for internal usage only.

RCKS [1:0]: RO calibration clock select:
[00]: 32XMDR **[01]:** 16MHz **[10]:** 8XMDR **[11]:** 4XMDR

MVS [1:0]: RO calibration moving average mode.
[00]: 1 [01]: 2 [10]: 4 [11]: 8

9.2.8 RC Target Control Register (Address: 0x50000048h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	TGNUM7	TGNUM6	TGNUM5	TGNUM4	TGNUM3	TGNUM2	TGNUM1	TGNUM0
R	NUMLH7	NUMLH6	NUMLH5	NUMLH4	NUMLH3	NUMLH2	NUMLH1	NUMLH0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W					TGNUM11	TGNUM10	TGNUM9	TGNUM8
R					NUMLH11	NUMLH10	NUMLH9	NUMLH8
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

TGNUM [11:0]: RO N Counter target (write only).
RO N Counter calibration goal or manual setting.

9.2.9 XRC Control I Register (Address: 0x50000050h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W			EKICR1	EKICR0	XRCS	ENRC	MXRC	XRCC
R								XRCC
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

EKICR[1:0]: Enable kick-off circuit select.
[00]:0us; [01]:10us; [1x]:20us.

XRCS: Main clock source select.
[0]: Crystal oscillator (External). **[1]:** XRC oscillator (Internal)

ENRC: Enable Internal XRC oscillator.
[0]: Disable. **[1]:** Enable.

MXRC: XRO bank manual calibration.
[0]: Disable. **[1]:** Enable.

XRCC: XRO bank calibration (Auto clear when done).

[0]: Disable. **[1]:** Enable.

9.2.10 XRC Control II Register (Address: 0x50000054h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	MTRIM7	MTRIM6	MTRIM5	MTRIM4	MTRIM3	MTRIM2	MTRIM1	MTRIM0
R	TRIM7	TRIM6	TRIM5	TRIM4	TRIM3	TRIM2	TRIM1	TRIM0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								MTRIM8
R								TRIM8
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W					CI1	CI0	ICONTROL1	ICONTROL0
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W							MVXS1	MVXS0
R								

MTRIM [8:0]: XRO Bank manual calibration value (write only).
Manual setting when MXRC =1.

TRIM [8:0]: XRO Bank auto calibration value (read only).

CI[1:0]: Reserved for internal usage only.

ICONTROL[1:0]: Reserved for internal usage only.

MVXS [1:0]: XRO calibration moving average mode.
[00]: 1 [01]: 2 [10]: 4 [11]: 8

9.2.11 XRC Target Control Register (Address: 0x50000058h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	XTGNUM7	XTGNUM6	XTGNUM5	XTGNUM4	XTGNUM3	XTGNUM2	XTGNUM1	XTGNUM0
R	NUMLH7	NUMLH6	NUMLH5	NUMLH4	NUMLH3	NUMLH2	NUMLH1	NUMLH0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W						XTGNUM10	XTGNUM9	XTGNUM8
R						NUMLH10	NUMLH9	NUMLH8
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

XTGNUM [10:0]: RO N Counter target (write only).
RO N Counter calibration goal or manual setting.

9.3 12bit ADC control register start at Address[31:0]= 50080000

Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
12 bit ADC Control	0x0000	W													CKS1	CKS0	DELS1	DELS0
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W	ADCIOS3	ADCIOS2	ADCIOS1	ADCIOS0			ADIVL	ADCYC	BUFS12B			MODE12	MVS122	MVS121	MVS120	ADCE12

		R												MODE12	MVS122	MVS121	MVS120	ADCE12
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
12 bit ADC	0x0004	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W																
		R					ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
Name	Offset		BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
12 bit ADC INTSTATE	0x0008	W																
		R																
			BIT 15	BIT14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		W																ADCI_Clear
		R																ADCI_STATE

9.3.1 12bit ADC Control Register (Address: 0x50080000h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	BUFS12B			MODE12	MVS122	MVS121	MVS120	ADCE12
R				MODE12	MVS122	MVS121	MVS120	ADCE12
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	ADCIOS3	ADCIOS2	ADCIOS1	ADCIOS0			ADIVL	ADCYC
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W					CKS1	CKS0	DELS1	DELS0
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

BUFS12B: buffer select for 12bit ADC.
[0]: deselect [1]: select.

MODE12: ADC 12bit mode.
[0]: one time. [1]: continuous.

MVS12B [2:0]: 12bit ADC moving average mode.
[000]:1, [001]:2, [010]:3, [011]:4, [100]:5, [101]:6, [110]:7, [111]:8

ADCE12: ADC 12bit measurement enable.
[0]: disable [1]: enable.

ADCIOS[3:0]: ADC I/O select.

ADIVL: ADC 12bit initial value.
[0]:0, [1]:2048.

ADCYC: ADC 12bit counter reference.
[0]:31 [1]: 32.

CKS[1:0]: ADC 12bit main clock select.
[00]:4M [01]: 2M. [10]:1M [11]: 0.5M.

DELS[1:0]: ADC 12bit measurement delay select.
[00]:5us [01]: 10us. [10]:15us [11]: 20us.

9.3.2 12bit ADC Register (Address: 0x500800004h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								
R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R					ADC11	ADC10	ADC9	ADC8
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

ADC12 [11:0]: ADC 12bit value.

9.3.3 12bit ADC INTSTATE Register (Address: 0x500800008h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								ADCI_Clear
R								ADCI_STATE
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

ADCI_Clear: ADC 12bit INT clear.
[0]:normal, [1]:clear.

ADCI_STATE: ADC 12bit INT State.

9.4 Flash memory controller register start at Address[31:0]= 4001F000

Flash mode register (Offset: 0x100)

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x100	R/W	RBB	TRIM	-	INF	TM[3]	TM[2]	TM[1]	TM[0]
Reset		1	0	0	0	0	0	0	0

TM[3:0] (Flash Test Mode enable)

INF (Flash Information page enable)
[1]: Enable
[0]: Disable

TRIM (Flash trim mode enable)

[1]: Enable
[0]: Disable

RBB (Flash Ready status output)
[1]: Ready
[0]: Not Ready.

Flash control register (Offset: 0x104)

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x104	R/W	CE			MERASE	SERASE	PERASE	PROG	WRONLY
Reset		1	0	0	0	0	0	0	0

WRONLY (Flash Page Write enable)
[1]: Enable
[0]: Disable

PROG (Flash Page Program internal Erase and Write enable)
[1]: Enable
[0]: Disable

PERASE (Flash Page Erase enable)
[1]: Enable
[0]: Disable

SERASE (Flash Sector Erase enable)
[1]: Enable
[0]: Disable

MERASE (Flash Mass Erase enable)
[1]: Enable
[0]: Disable

CE (Flash chip enable)
[1]: Enable
[0]: Disable

Flash pwe register (Offset: 0x108)

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x108	R/W	PWE		PWE_L[5]	PWE_L[4]	PWE_L[3]	PWE_L[2]	PWE_L[1]	PWE_L[0]
Reset		0	0	0	0	0	0	0	0

PWE (Flash IAP program enable)
[1]: Enable
[0]: Disable

PWE_L[5:0](Flash IAP program length)
[000001]: 1 double word.
[000010]: 2 double word.
...
[100000]: 32 double word.

Flash pwe start address register (Offset: 0x10C)

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x10C	R/W	PWE_A[7]	PWE_A[6]	PWE_A[5]	PWE_A[4]	PWE_A[3]	PWE_A[2]	PWE_A[1]	PWE_A[0]
Reset		0	0	0	0	0	0	0	0

Offset	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x10D	R/W	PWE_A[15]	PWE_A[14]	PWE_A[13]	PWE_A[12]	PWE_A[11]	PWE_A[10]	PWE_A[9]	PWE_A[8]
Reset		0	0	0	0	0	0	0	0

Offset	R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0x10E	R/W	PWE_A[23]	PWE_A[22]	PWE_A[21]	PWE_A[20]	PWE_A[19]	PWE_A[18]	PWE_A[17]	PWE_A[16]
Reset		0	0	0	0	0	0	0	0

Offset	R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0x10F	R/W	PWE_A[31]	PWE_A[30]	PWE_A[29]	PWE_A[28]	PWE_A[27]	PWE_A[26]	PWE_A[25]	PWE_A[24]
Reset		0	0	0	0	0	0	0	0

PWE_A[31:0](Flash IAP program start address)

Flash pwe program data register (Offset: 0x200~0x27F)

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x200	R/W	PWE_D0[7]	PWE_D0[6]	PWE_D0[5]	PWE_D0[4]	PWE_D0[3]	PWE_D0[2]	PWE_D0[1]	PWE_D0[0]
Reset		0	0	0	0	0	0	0	0

Offset	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x201	R/W	PWE_D0[15]	PWE_D0[14]	PWE_D0[13]	PWE_D0[12]	PWE_D0[11]	PWE_D0[10]	PWE_D0[9]	PWE_D0[8]
Reset		0	0	0	0	0	0	0	0

Offset	R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0x202	R/W	PWE_D0[23]	PWE_D0[22]	PWE_D0[21]	PWE_D0[20]	PWE_D0[19]	PWE_D0[18]	PWE_D0[17]	PWE_D0[16]
Reset		0	0	0	0	0	0	0	0

Offset	R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0x203	R/W	PWE_D0[31]	PWE_D0[30]	PWE_D0[29]	PWE_D0[28]	PWE_D0[27]	PWE_D0[26]	PWE_D0[25]	PWE_D0[24]
Reset		0	0	0	0	0	0	0	0

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x204	R/W	PWE_D1[7]	PWE_D1[6]	PWE_D1[5]	PWE_D1[4]	PWE_D1[3]	PWE_D1[2]	PWE_D1[1]	PWE_D1[0]

Reset		0	0	0	0	0	0	0	0

Offset	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x205	R/W	PWE_D1[15]	PWE_D1[14]	PWE_D1[13]	PWE_D1[12]	PWE_D1[11]	PWE_D1[10]	PWE_D1[9]	PWE_D1[8]
Reset		0	0	0	0	0	0	0	0

Offset	R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0x206	R/W	PWE_D1[23]	PWE_D1[22]	PWE_D1[21]	PWE_D1[20]	PWE_D1[19]	PWE_D1[18]	PWE_D1[17]	PWE_D1[16]
Reset		0	0	0	0	0	0	0	0

Offset	R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0x207	R/W	PWE_D1[31]	PWE_D1[30]	PWE_D1[29]	PWE_D1[28]	PWE_D1[27]	PWE_D1[26]	PWE_D1[25]	PWE_D1[24]
Reset		0	0	0	0	0	0	0	0

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x208	R/W	PWE_D2[7]	PWE_D2[6]	PWE_D2[5]	PWE_D2[4]	PWE_D2[3]	PWE_D2[2]	PWE_D2[1]	PWE_D2[0]
Reset		0	0	0	0	0	0	0	0

Offset	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x209	R/W	PWE_D2[15]	PWE_D2[14]	PWE_D2[13]	PWE_D2[12]	PWE_D2[11]	PWE_D2[10]	PWE_D2[9]	PWE_D2[8]
Reset		0	0	0	0	0	0	0	0

Offset	R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0x20A	R/W	PWE_D2[23]	PWE_D2[22]	PWE_D2[21]	PWE_D2[20]	PWE_D2[19]	PWE_D2[18]	PWE_D2[17]	PWE_D2[16]
Reset		0	0	0	0	0	0	0	0

Offset	R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0x20B	R/W	PWE_D2[31]	PWE_D2[30]	PWE_D2[29]	PWE_D2[28]	PWE_D2[27]	PWE_D2[26]	PWE_D2[25]	PWE_D2[24]
Reset		0	0	0	0	0	0	0	0

….

Offset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x27C	R/W	PWE_D1F[7]	PWE_D1F[6]	PWE_D1F[5]	PWE_D1F[4]	PWE_D1F[3]	PWE_D1F[2]	PWE_D1F[1]	PWE_D1F[0]
Reset		0	0	0	0	0	0	0	0

Offset	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x27D	R/W	PWE_D1F[15]	PWE_D1F[14]	PWE_D1F[13]	PWE_D1F[12]	PWE_D1F[11]	PWE_D1F[10]	PWE_D1F[9]	PWE_D1F[8]
Reset		0	0	0	0	0	0	0	0

Offset	R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0x27E	R/W	PWE_D1F[23]	PWE_D1F[22]	PWE_D1F[21]	PWE_D1F[20]	PWE_D1F[19]	PWE_D1F[18]	PWE_D1F[17]	PWE_D1F[16]
Reset		0	0	0	0	0	0	0	0

Offset	R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0x27F	R/W	PWE_D1F[31]	PWE_D1F[30]	PWE_D1F[29]	PWE_D1F[28]	PWE_D1F[27]	PWE_D1F[26]	PWE_D1F[25]	PWE_D1F[24]
Reset		0	0	0	0	0	0	0	0

PWE_D0[31:0](Flash IAP program data of start address)
PWE_D1[31:0](Flash IAP program data of start address+1)
PWE_D2[31:0](Flash IAP program data of start address+2)
…
PWE_D1F[31:0](Flash IAP program data of start address+32)

10. SOC Architectural Overview

A8137M0 microcontroller is instruction set compatible with Cortex™-M0 profile processors. Besides FSK/GFSK RF transceiver, A8137M0 integrates many features, three 8/16bit counters/timers, watchdog timer, RTC, UART, SPI interface, I^2C interface, 8 channels PWM, 4 channels ADC and battery detector, The interrupt controller is extended to support 10 interrupt sources; UART, Timer, watchdog timer, IO prot, SPI, I^2C, ADC and RF. A8137M0 includes JTAG (2-wire) debug circuitry that provides full time, real-time, in-circuit debugging.

10.1 ARM Cortex-M0

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex™-M0 profile processors. The profile supports two MODEs - Thread MODE and Handler MODE. Handler MODE is entered as a result of an exception. An exception return can only be issued in Handler MODE. Thread MODE is entered on Reset and can be entered as a result of an exception return. The following figure shows the functional controller of the processor.

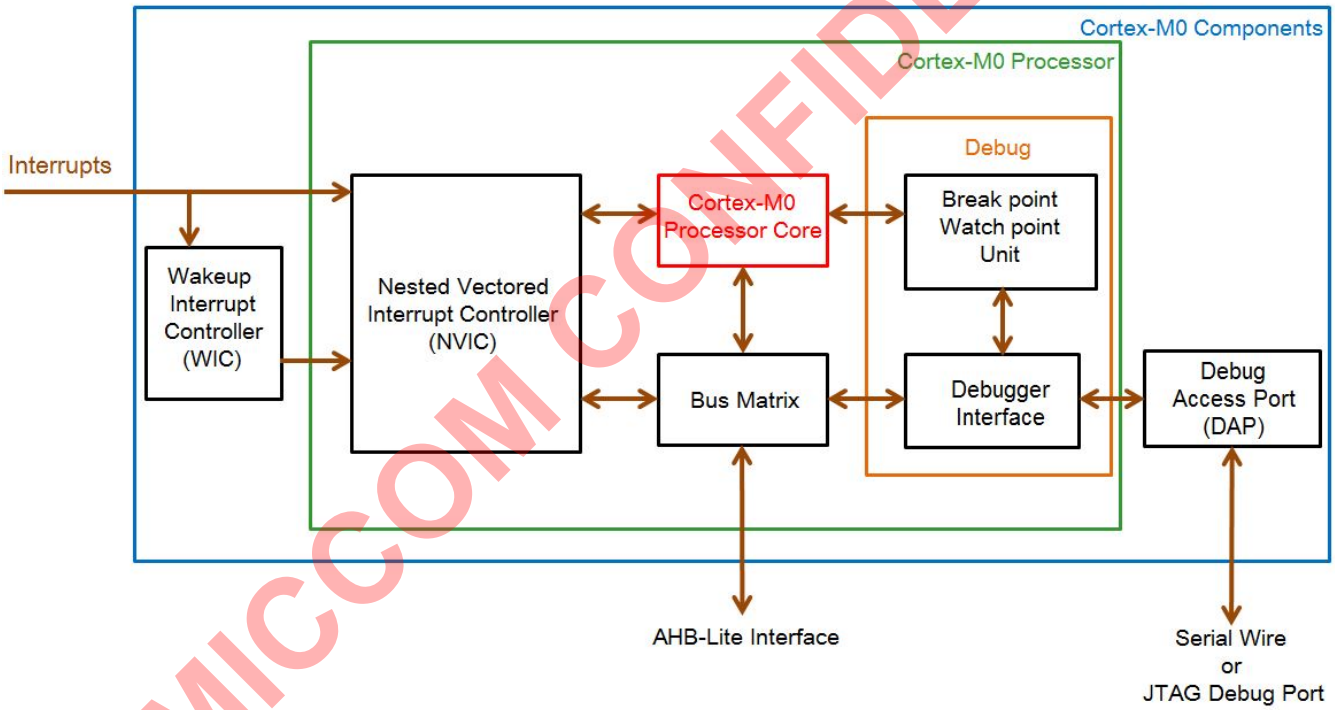


Figure 10.1 Core-M0 block diagram

10.1.1 Feature

- A low gate count processor
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception MODEl:
    This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception MODEl that enables the use of pure C functions as interrupt handlers

- Low power Idle MODE entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature

- NVIC
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Idle MODE
- Debug support
  - Four hardware breakpoints
  - Two watch points
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

10.2 Memory Organization

The memory organization is shown as figure 10.2

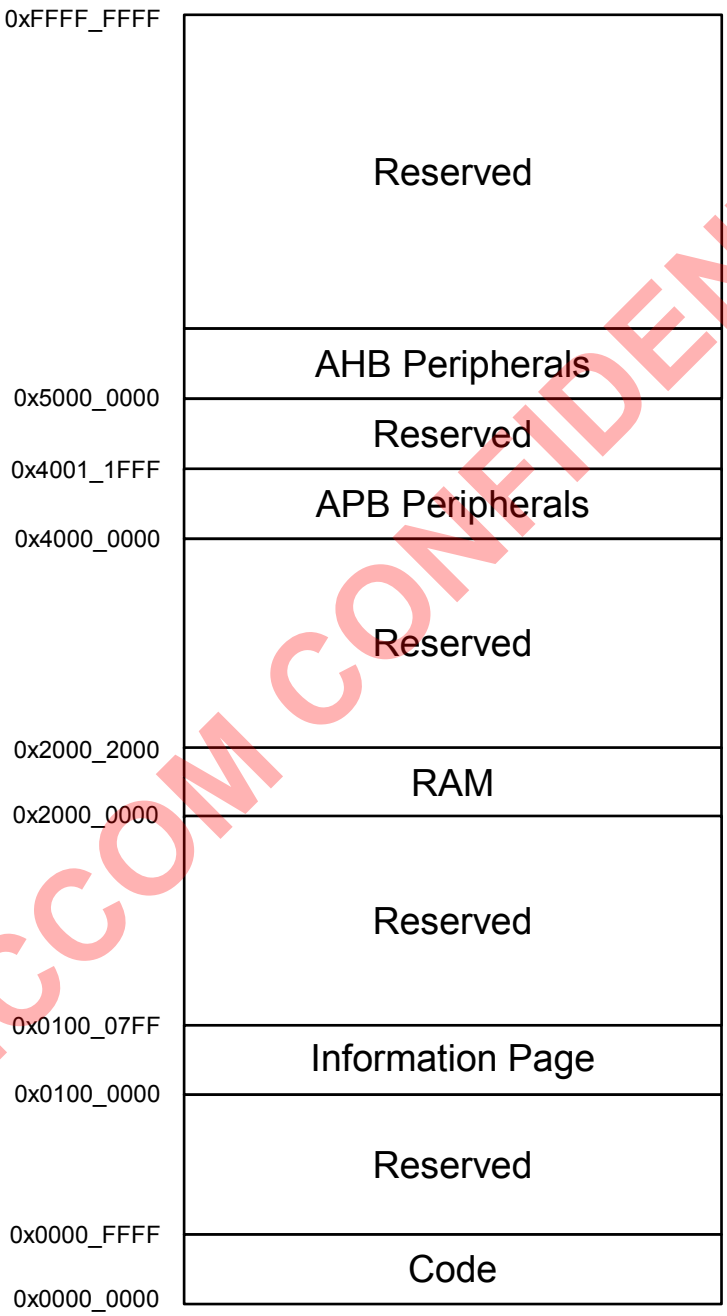


Figure 10.2 Memory Organization

10.3 Nested Vectored Interrupt Controller (NVIC)

The Cortex™-M0 CPU provides an interrupt controller as an integral part of the exception MODE, named as "Nested Vectored Interrupt Controller (NVIC)", which is closely coupled to the processor core and provides following features.

10.3.1 Feature

- Flexible interrupt management

In the Cortex-M0 processor, each external interrupt can be enabled or disabled and can have its pending status set or clear by software. It can also accept exception requests at signal level (interrupt request from a peripheral remain asserted until the interrupt service routine clears the interrupt request), as well as an exception request pulse (minimum 1 clock cycle). This allows the interrupt controller to be used with any interrupt source.

- Nested interrupt support

In the Cortex-M0 processor, each exception has a priority level. The priority level can be fixed or programmable. When an exception occurs, such as an external interrupt, the NVIC will compare the priority of this exception to the current level. If the new exception has a higher priority, the current running task will be suspended. Some of the registers will be stored on to the stack memory, and the processor will start executing the exception handler of the new exception. This process is called "preemption." When the higher priority exception handler is complete, it is terminated with an exception return operation and the processor automatically restores the registers from the stack and resumes the task that was running previously. This mechanism allows nesting of exception services without any software overhead.

- Vectored exception entry

When an exception occurs, the processor will need to locate the starting point of the corresponding exception handler. Traditionally, in ARM processors such as the ARM7TDMI, software usually handles this step. The Cortex-M0 automatically locates the starting point of the exception handler from a vector table in the memory.
As a result, the delay from the start of the exception to the execution of the exception handlers is reduced.

- Interrupt masking

The NVIC in the Cortex-M0 processor provides an interrupt masking feature via the PRIMASK special register. This can disable all exceptions except hard fault and NMI. This masking is useful for operations that should not be interrupted such as time critical control tasks or real-time multimedia codecs.

10.3.2 Exception Types and Interrupt Map

Each exception source in the Cortex-M0 processor has a unique exception number. The exception number for NMI is 2, and the exception numbers for the on-chip peripherals and external interrupt sources are from 16 to 47. The other exception numbers, from 1 to 15, are for system exceptions generated inside the processor, although some of the exception numbers in this range are not used. Each exception type also has an associated priority. The priority levels of some exceptions are fixed and some are programmable. Table 8.1 shows the exception types, exception numbers, and priority levels.

Exception Number	Exception Type	Priority	Interrupt Description
1	Reset	-3(Highest)	Reset
2	NMI	-2	Non maskable interrupt
3	Hard fault	-1	Fault handing exception
4-10	Reserved	--	--
11	SVC	Programmable	Supervisor call via SVC instruction
12-13	Reserved	--	--
14	PendSV	Programmable	Pendable request for system service
15	SysTick	Programmable	System tick timer
16-47	IRQ0~IRQ31	Programmable	IRQ

Table 10.1 Exceptions Type

Exception Number	Interrupt Number Bit	Interrupt Name	Interrupt Description
16	0	--	-
17	1	UART0_INT	UART0 Tx/Rx/Overflow interrupt
18	2	--	--
19	3	RADIO_INT	RADIO interrupt
20	4	--	--
21	5	UART2_INT	UART2 Tx/Rx/Overflow interrupt
22	6	PORT0_COMB_INT	GPIO 0 combined/Key interrupt
23	7	--	--
24	8	TIMER0	Timer0 interrupt
25	9	TIMER1	Timer1 interrupt
26	10	Dual_Timer_INT	Dual Timer interrupt
27	11	--	--
28	12	--	--
29	13	UART1_INT	UART1 Tx/Rx/Overflow interrupt
30	14	--	--
31	15	--	--
32	16	SPI_INT	SPI interrupt
33	17	I^2C_INT	I^2CM/I^2CS interrupt
34	18	--	--
35	19	--	--
36	20	--	--
37	21	ADC_INT	12bits-ADC interrupt
38	22	--	--
39	23	--	--
40	24	--	--
41	25	--	--
42	26	--	--
43	27	--	--
44	28	--	--
45	29	--	--
46	30	--	--
47	31	--	--

Table 10.2 Interrupt Map Vector Table

10.4 Reset source

Reset circuitry allows A8137M0 to be easily placed in a predefined default condition. LVD, Reset, POR, and Watchdog signal will reset A8137M0 when they happen.

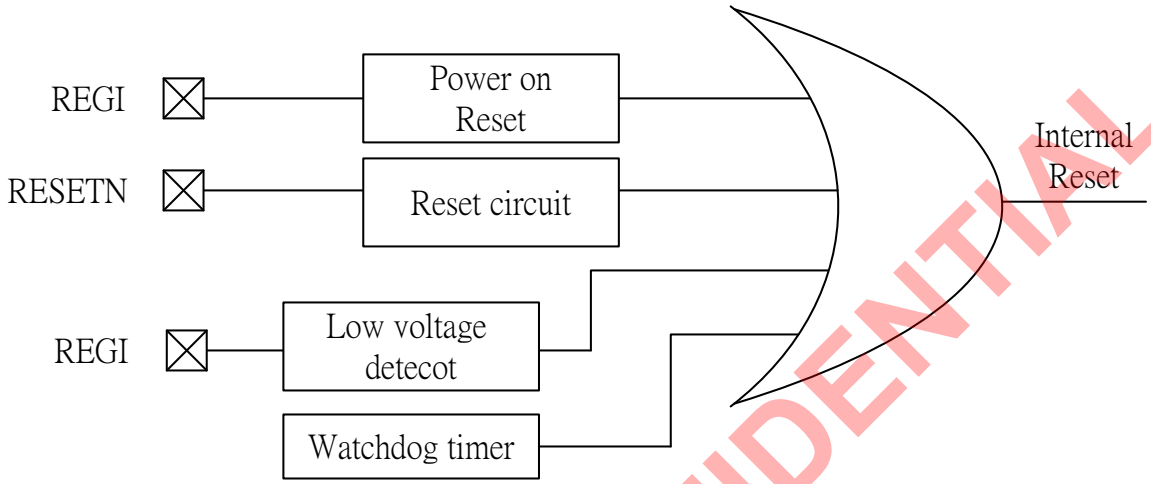


Figure 10.3 Reset source

10.4.1 Power Control I Register (Address: 0x50000008h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W				PM1S-	-QD	REGAE	PM3F	STOP
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W					CLKSEL2	CLKSEL1	CLKSEL0	PMM
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	PD_LVD					BODFCLR	RESTFCLR	PORFCLR
R						BODF	RESETNF	PORF
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

PORF (power-on reset flag)
= 1: Occurred Power-on Reset
= 0: No Power-on Reset
PORFCLR write 1 to clear.

RESETNF (RESETN flag)
= 1: Occurred RESETN reset
= 0: No RESETN reset
RESTFCLR write 1 to clear.

LVD (Low voltage detect) flag
= 1: Occurred Low Voltage Reset
= 0: No Low Voltage reset
BODFCLR write 1 to clear.

10.5 Clock source

A8137M0 has three clock source, crystal oscillator (pin 15,16/ Xi, XO), RTC crystal (pin 43,44/ P0.22, P0.23/ RTC_I, RTC_O) and internal RC oscillator. In the MCU part (digital peripherals), user choices the suitable clock source by power consumptions and performance. In the RF part, the clock source only comes from XO..

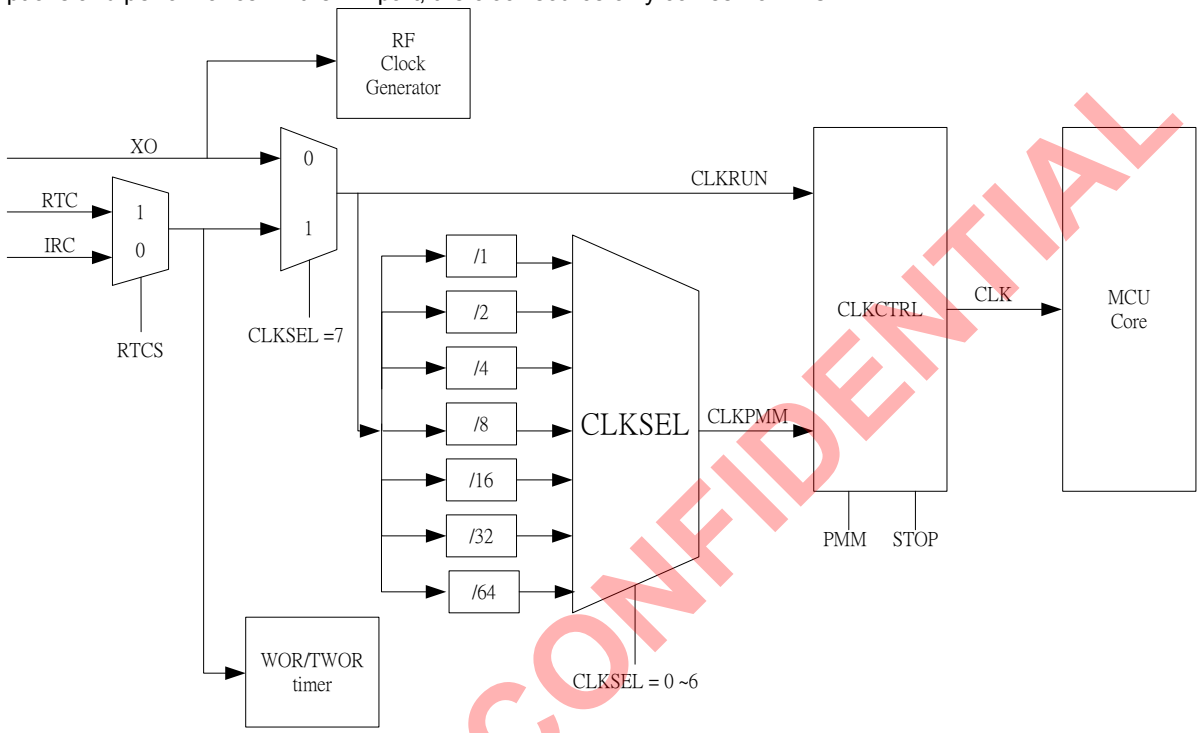


Figure 10.4 Whole chip clock

10.6 System Timer (SysTick)

The SysTick timer is a 24-bit down counter. It reloads automatically after reaching zero, and the reload value is programmable. When reaching zero, the timer can generate a SysTick exception (exception number 15). For the Cortex-M0 processor, a simple timer called the SysTick is included to generate this regular interrupt request.

10.6.1 SysTick Control and Status Register (Address: 0xE000E010h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W						CLKSOURCE	TICKINT	ENABLE
R						CLKSOURCE	TICKINT	ENABLE
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								COUNTFLAG
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

COUNTFLAG Returns 1 if timer counted to 0 since the last read of this register.
CLKSOURCE Selects the SysTick timer clock source
0 = external reference clock
1 = processor clock.
If your device does not implement a reference clock, this bit reads-as-one and ignores writes.
TICKINT Enables SysTick exception request:
0 = counting down to zero does not assert the SysTick exception request

1 = counting down to zero to asserts the SysTick exception request.
ENABLE Enables the counter:
0 = counter disabled
1 = counter enabled.

10.6.2 SysTick Reload Value Register (Address: 0xE000E014h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD
R	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD
R	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD
R	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

RELOAD Value to load into the SYST_CVR when the counter is enabled and when it reaches 0, see Calculating the RELOAD value.

10.6.3 SysTick Current Value Register (Address: 0xE000E018h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT
R	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT
R	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT
R	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT	CURRENT
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

CURRENT Reads return the current value of the SysTick counter.

10.6.4 SysTick Calibration Value Register (Address: 0xE000E01Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								
R	TENMS	TENMS	TENMS	TENMS	TENMS	TENMS	TENMS	TENMS
R/W			**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R	TENMS	TENMS	TENMS	TENMS	TENMS	TENMS	TENMS	TENMS
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R	TENMS	TENMS	TENMS	TENMS	TENMS	TENMS	TENMS	TENMS
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R	NOREF	SKEW						

NOREF Indicates whether the device provides a reference clock to the processor:
0 = reference clock provided
1 = reference clock provided.
If your device does not provide a reference clock, the SYST_CSR.CLKSOURCE bit reads-as-one and ignores writes.
SKEW Indicates whether the TENMS value is exact:
0 = TENMS value is exact
1 = TENMS value is inexact, or not given.

An inexact TENMS value can affect the suitability of SysTick as a software real time clock.
TENMS Reload value for 10ms (100Hz) timing, subject to system clock skew errors.
If the value reads as zero, the calibration value is not known.
If calibration information is not known, calculate the calibration value required from the frequency of the processor clock or external clock.

11. I/O Ports

A8137M0 has 24pins digital I/O Pins and each of the Port pin can be defined as general-purpose I/O (GPIO) or peripheral I/O signals connected to the timers, UART, I^2C and SPI functions. Thus, each pin can also be used to wake up from sleep MODE. User can select each pin function by setting register. Each port has itself port register like P0 (0x40010000), that are both byte addressable and bit addressable. When reading, the logic levels of the Port's input pins are returned. Each port has three registers to setting Pull-up (PUN), Output-enable (OE) and Wake-up enable (WUN). As shown the bellow block diagram, Fig. 11.1. Unused I/O pins should have a defined level and not be left floating. One way to do this is to leave the pin unconnected and configure the pin as a general-purpose I/O input with pull-up resistor.

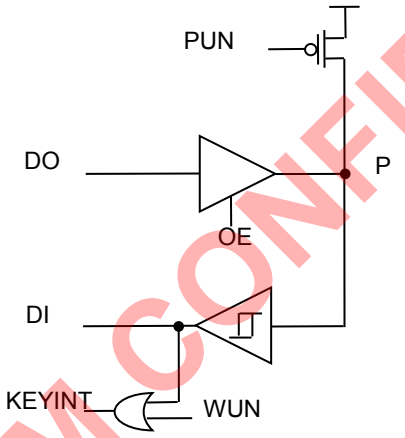


Figure11.1 Ports I/O block diagram

OE	PUN	P	DI
0	0	1	1
0	1	HZ	INH
1	X	DO	DO

Table 11.1 OE and PUN setting and Output(P) and Input(DI)

11.1 FUNCTIONALITY

According the Table 11.1, all Port pins can be configured as Output, Input with the pull-up resistor (around 100 Kohm) or Input. Please refer the following truth table to know every function setting. When OE=1, this pin is configured as Output. Otherwise OE =0, this pin is configured as Input. User can set PUN =1 or 0 depending on application. When OE =0, PUN=0 is recommended for saving power.

All Port pins can wake A8137M0 up when WUEN=0 and configured GPIO. All Port pins' WUN signals connect one OR gate to KEYINT. It means pin wake up function needs KEYINT ISR to take care this interrupt event.

Some IO pin have multiple function, like as UART, SPI, I^2C, PWM, Timer and RF, that can enabled by ALTFUNCEN when User need used one of them. The IO mapping refer to Chapter 5, please.

11.1.1 Pull up Register (Address: 0x40010004h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

W	PUN	PUN	PUN	PUN	PUN	PUN	PUN	PUN
R	PUN	PUN	PUN	PUN	PUN	PUN	PUN	PUN
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	PUN	PUN	PUN	PUN	PUN	PUN	PUN	PUN
R	PUN	PUN	PUN	PUN	PUN	PUN	PUN	PUN
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	PUN	PUN	PUN	PUN	PUN	PUN	PUN	PUN
R	PUN	PUN	PUN	PUN	PUN	PUN	PUN	PUN
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

PUN IO input pull up when PUN = 0

11.1.2 Output Enable Register (Address: 0x4001000Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	OE	OE	OE	OE	OE	OE	OE	OE
R	OE	OE	OE	OE	OE	OE	OE	OE
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	OE	OE	OE	OE	OE	OE	OE	OE
R	OE	OE	OE	OE	OE	OE	OE	OE
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	OE	OE	OE	OE	OE	OE	OE	OE
R	OE	OE	OE	OE	OE	OE	OE	OE
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

OE IO output enable when OE = 1

11.1.3 Alternative Function Enable Register (Address: 0x40010018h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET
R	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET
R	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET
R	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET	ALTFUNCSET
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

ALTFUNCSET write 1 to set ALTFUNCSET

11.2 GPIO interrupt

A8137M0 support all pin interrupt, that offer level / edge interrupt trigger and polarity select. User can use P0 port as key input and meanwhile these key are clicked to event a key interrupt to enter key process flow or setting WUN to wake up A8137M0. It's more helpful to design a remote controller and low power consumption with power saving MODE setting.

The KEY interrupts can wake up A8137M0 back to normal MODE in PM1 and PM2. In PM3, Port 0.18~Port 0.23 and RESETN PIN will reset A8137M0 and A8137M0 need to initial all needed peripherals and take care key interrupt event.

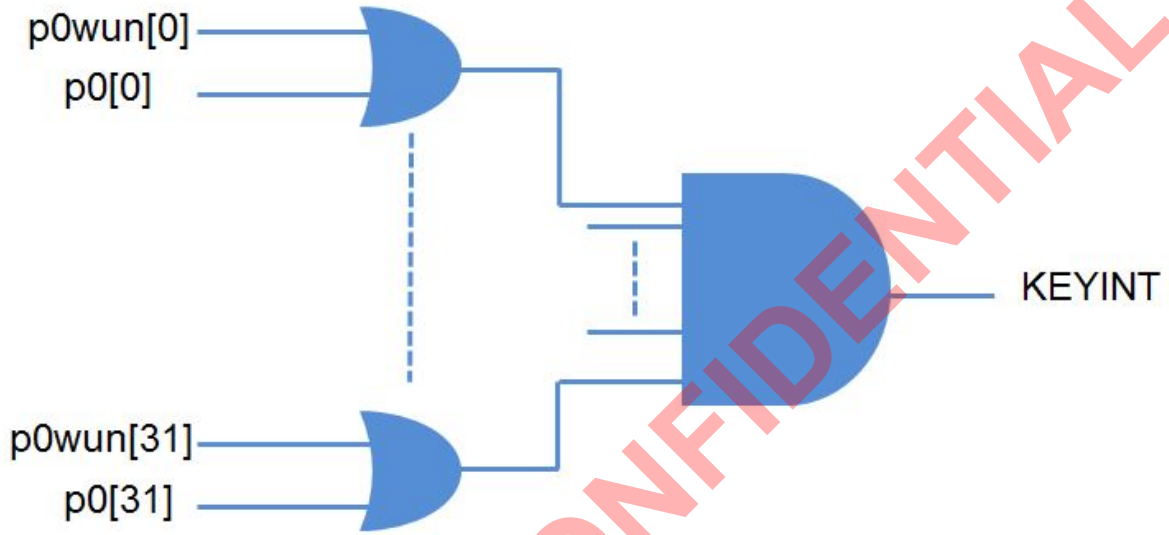


Figure11.2 Key interrupt block diagram

11.2.1 Wake up Register (Address: 0x4001000Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	WUN	WUN	WUN	WUN	WUN	WUN	WUN	WUN
R	WUN	WUN	WUN	WUN	WUN	WUN	WUN	WUN
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	WUN	WUN	WUN	WUN	WUN	WUN	WUN	WUN
R	WUN	WUN	WUN	WUN	WUN	WUN	WUN	WUN
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	WUN	WUN	WUN	WUN	WUN	WUN	WUN	WUN
R	WUN	WUN	WUN	WUN	WUN	WUN	WUN	WUN
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

WUN Wake up interrupt enable when WUN = 1, and WUN=0 for disable.

11.2.2 Interrupt Enable Register (Address: 0x40010020h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN
R	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN
R	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN
R	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN	INTSEN
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-

R	-	-	-	-	-	-	-	-

INTEN write 1 to enable pint interrupt.

11.2.3 Interrupt Type Enable Register (Address: 0x40010028h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET
R	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET
R	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET
R	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET	INTTYPESET
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

INTTYPESET Interrupt type select
[0]: For level trigger
[1]: For edge trigger

11.2.4 Interrupt Polarity Register (Address: 0x40010030h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET
R	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET
R	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET
R	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET	INTPOLSET
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

INTPOLSET Interrupt polarity select
[0]: For low level / falling edge trigger
[1]: For high level / rising edge trigger

12. Timer 0 & 1

A8137M0 contains two 32-bit timer/counters, Timer 0 and Timer 1. Timer 0 and Timer 1 in the “timer mode“, the period depend on VALUE (Offset: 0x0004) and RELOAD (Offset: 0x0008) setting, when appropriate timer is enabled. In the “counter mode” the timer registers are incremented every falling transition on theirs corresponding input pins: Timer0_EIN (P0.8) or Timer1_EIN (P0.9). The input pins are sampled every CLK period.

PIN	ACTIVE	TYPE	DESCRIPTION
Timer0_EIN (P0.8)	Riseing edge	Input	external input as clock
	High level		external input as enable
Timer1_EIN (P0.9)	Riseing edge	Input	external input as clock
	High level		external input as enable

12.1 Overview

- An interrupt request signal, **TIMERINT,** when the counter reaches 0.
  The interrupt request is held until it is cleared by writing to the INTCLEAR Register
- If the timer count reaches 0 and, at the same time, the software clears a previous interrupt status, the interrupt status is set to 1.
- A timer enable, **EXTIN(P0_8/P0_9),** can use the zero to one transition of the external input signal
- The external clock, **EXTIN**, must be slower than half of the peripheral clock because it is sampled by a double flip-flop and then goes through edge-detection logic when the external inputs act as a clock

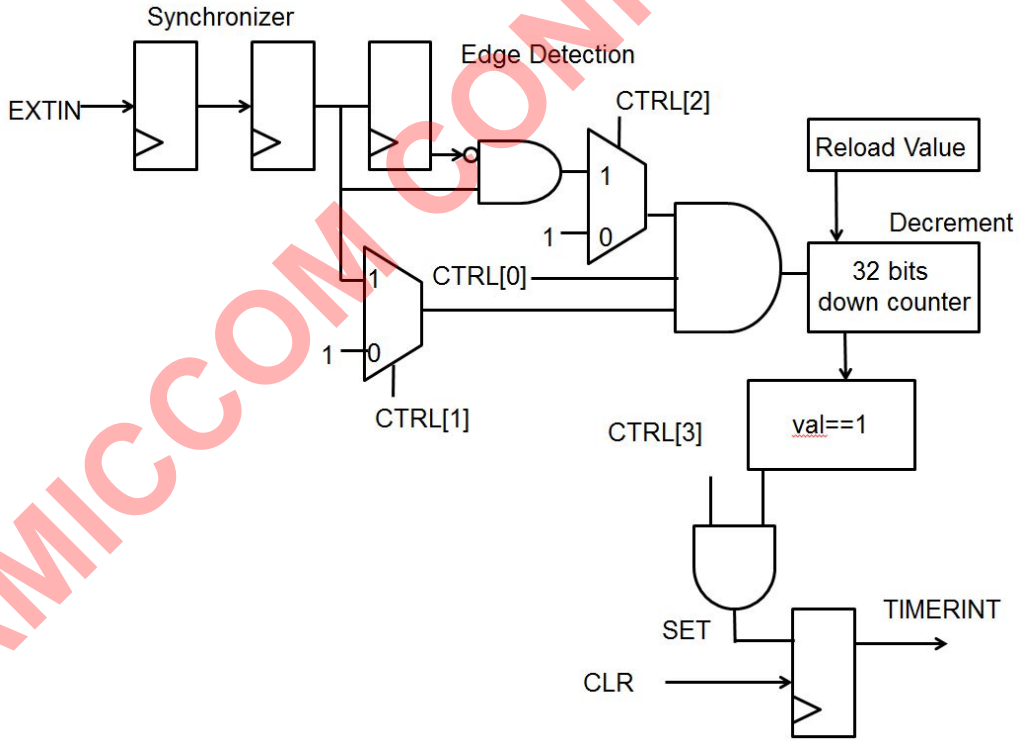


Figure12.1 Timer 32-Bit Timer/Counter

12.1.1 Timer control register (Address: 0x40000000h, 0x40001000h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W					CTRL3	CTRL2	CTRL1	CTRL0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

CTRL0 Enable.
CTRL1 Select external input as enable.
CTRL2 Select external input as clock.
CTRL3 Timer interrupt enable.

12.1.2 Value Register (Address: 0x40000004h, 0x40001004h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE
R	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE
R	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE
R	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE
R	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE

VALUE Current value

12.1.3 Reload Register (Address: 0x40000008h, 0x40001008h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD
R	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD
R	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD
R	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD
R	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD	RELOAD

RELOAD Reload value. Set the current value.

12.1.4 Interrupt State Register (Address: 0x4000000Ch, 0x4000100Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								INTCLEAR
R								INTSTATUS
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

INTSTATUS Timer interrupt.
= 1: Occurred Timer interrout
INTCLEAR write 1 to clear

13. Dual Timer

A8137M0 contains two 32-bit down-counters., dual-input timer module, is an APB slave module consisting of two programmable 32-bit down-counters that can generate interrupts when they reach 0.

13.1 Dual Timer FUNCTIONALITY

Two timers are defined by default, although you can easily expand this using extra instantiations of the FRC block. The same principle of simple expansion is used for the register configuration, to enable you to use more complex counters. For each timer, the following MODEs of operation are available:

- **Free-running MODE**
  The counter wraps after reaching its zero value, and continues to count down from the maximum value. This is the default MODE.

- **Periodic timer MODE**
  The counter generates an interrupt at a constant interval, reloading the original value after wrapping past zero.

- **One-shot timer MODE**
  The counter generates an interrupt once. When the counter reaches 0, it halts until you reprogram it. You can do this using one of the following:
  - Clearing the one-shot count bit in the control register, in which case the count proceeds according to the selection of Free-running or Periodic MODE.
  - Writing a new value to the Load Value register.

13.2 Dual Timer Operation

Each timer has an identical set of registers The operation of each timer is identical. The timer is loaded by writing to the load register and, if enabled, counts down to 0. When a counter is already running, writing to the load register causes the counter to immediately restart at the new value. Writing to the background load value has no effect on the current count. The counter continues to decrement to 0, and then restarts from the new load value, if in periodic MODE, and one-shot MODE is not selected.

When 0 is reached, an interrupt is generated. You can clear the interrupt by writing to the clear register. If you selected one-shot MODE, the counter halts when it reaches 0 until you deselect one-shot MODE, or write a new load value.

Otherwise, after reaching a zero count, if the timer is operating in free-running MODE, it continues to decrement from its maximum value. If you selected periodic timer MODE, the timer reloads the count value from the Load Register and continues to decrement. In this MODE, the counter effectively generates a periodic interrupt.

You select the MODE using a bit in the Timer Control Register. At any point, you can read the current counter value from the Current Value Register. You can enable the counter using a bit in the Control Register.

At reset, the counter is disabled, the interrupt is cleared, and the load register is set to 0. The MODE and prescale values are set to free-running, and clock divide of one respectively. Figure 13.1 shows a block diagram of the free-running timer module.

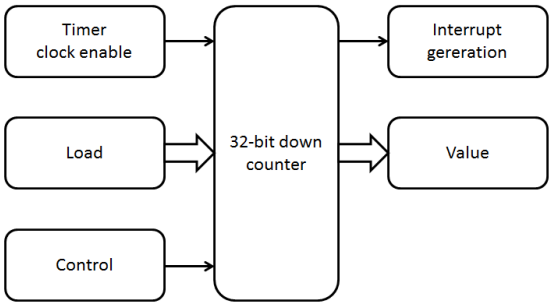


Figure13.1 Timer 32-Bit Timer/Counter

The timer clock enable is generated by a prescale unit. The counter then uses the enable to create a clock with one of the following timings:

- The system clock.
- The system clock divided by 16, generated by 4 bits of prescale.
- The system clock divided by 256, generated by 8 bits of prescale.

Figure 13.2 shows how the timer clock frequency is selected in the prescale unit. This enables you to clock the timer at different frequencies.

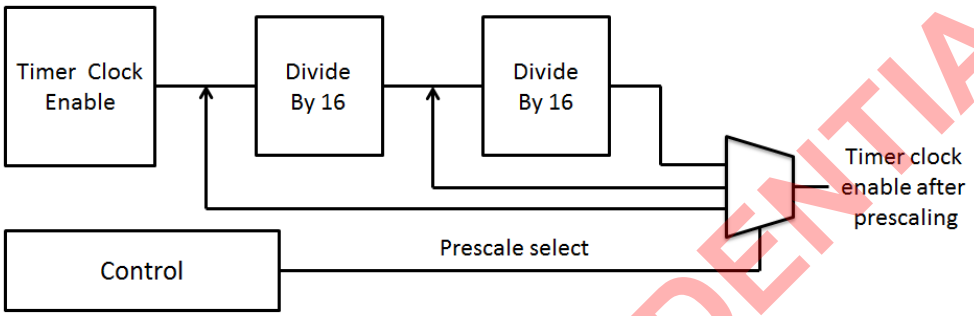


Figure13.2 Timer 32-Bit Timer/Counter

Interrupt generation

An interrupt is generated when the full 32-bit counter reaches 0, and is only cleared when the TimerXClear location is written to. A register holds the value until the interrupt is cleared. The most significant carry bit of the counter detects the counter reaching 0.

You can mask interrupts by writing 0 to the Interrupt Enable bit in the Control Register. You can read the following from status registers:

- Raw interrupt status, before masking.
- Final interrupt status, after masking.

The interrupts from the individual counters, after masking, are logically ORed into a combined interrupt, **TIMINTC**. This provides an additional output from the timer peripheral.

13.2.1 Timer Load Register (Address: 0x40002000h, 0x40002020h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD
R	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD
R	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD
R	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD
R	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD	LOAD

LOAD Timer 1/2 Load.

13.2.2 Timer Value Register (Address: 0x40002004h, 0x40002024h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE
R	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE
R	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**

W	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE
R	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE
R	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE	VALUE

VALUE Timer 1/2 value.

13.2.3 Timer control register (Address: 0x40002008h, 0x40002028h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	Timer Enable	Timer Mode	INT_EN		Pre_Prescale	Pre_Prescale	Slt	OS
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

Timer Eable Timer 1/2 enable.
[0]: disable.
[1]: enable.

Timer Mode Timer 1/2 MODE.
[0]: free-running MODE.
[1]: periodic MODE.

INT_EN Timer 1/2 interrupt enable.
[0]: timer interrupt disable.
[1]: timer interrupt enable.

Pre_Precale Timer 1 prescale.
[00]: 0 stages of prescale, clock is divided by 1.
[01]: 4 stages of prescale, clock is divided by 16
[10]: 8 stages of prescale, clock is divided by 256
[11]: Undefined

Slt Timer 1/2 size selects 16-bit or 32-bit counter operation
[0]: 16-bit counter
[1]: 32-bit counter

OS Timer 1/2 one-shot count selects
[0]: Wrapping MODE
[1]: One-shot MODE

13.2.4 Timer Interrupt Clear register (Address: 0x4000200Ch, 0x4000202Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	INTC	INTC	INTC	INTC	INTC	INTC	INTC	INTC
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**

W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

INTC Timer 1/2 interrupt clear

13.2.5 Timer Raw Interrupt State register (Address: 0x40002010h, 0x40002030h)

R/W	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
W								
R	RIS	RIS	RIS	RIS	RIS	RIS	RIS	RIS
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

RIS: Raw timer interrupt status from the counter.

13.2.6 Timer Interrupt Enable State register (Address: 0x40002014h, 0x40002034h)

R/W	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
W								
R	MIS	MIS	MIS	MIS	MIS	MIS	MIS	MIS
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

MIS Timer interrupt enabled status from the counter.

13.2.7 Timer BG Load register (Address: 0x40002018h, 0x40002038h)

R/W	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
W	BGL	BGL	BGL	BGL	BGL	BGL	BGL	BGL
R	BGL	BGL	BGL	BGL	BGL	BGL	BGL	BGL
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	BGL	BGL	BGL	BGL	BGL	BGL	BGL	BGL
R	BGL	BGL	BGL	BGL	BGL	BGL	BGL	BGL
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	BGL	BGL	BGL	BGL	BGL	BGL	BGL	BGL
R	BGL	BGL	BGL	BGL	BGL	BGL	BGL	BGL
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	BGL	BGL	BGL	BGL	BGL	BGL	BGL	BGL
R	BGL	BGL	BGL	BGL	BGL	BGL	BGL	BGL

BGL[31:0]: Timer 1/2 BG load.

14. UART 0 & 1

A8137M0 contains three UART, UART 0(P0.16/P0.17), UART 1(P0.18/P0.19), The APB UART, is a simple design that supports 8-bit communication without parity, and is fixed at one stop bit per configuration. Figure 14.1 shows the APB UART module

14.1 Overview

The APB UART contains buffering

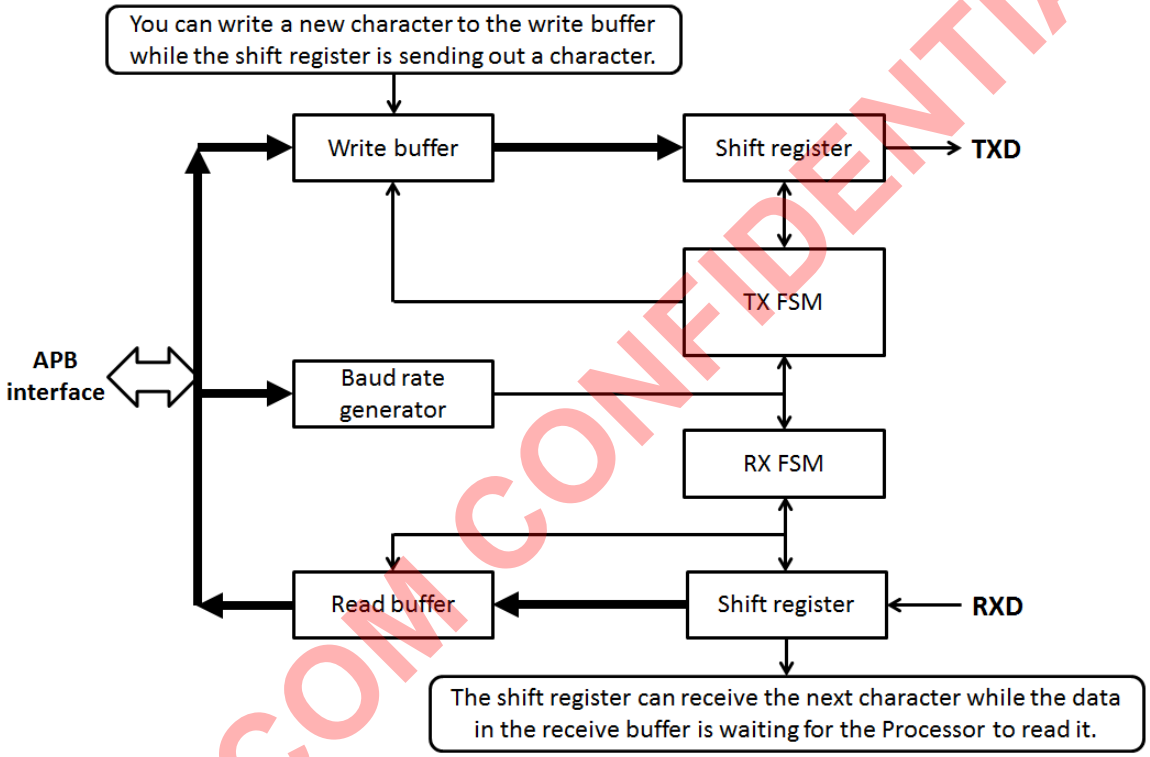


Figure 14.1 APB UART module.

PIN	ACTIVE	TYPE	DESCRIPTION
Rxd_0(P0.16)	-	Input / Output	Serial receiver I_0 / O_0
Txd_0(P0.17)	-	Output	Serial transmitter line 0

Table14.1 UART0 pins description

PIN	ACTIVE	TYPE	DESCRIPTION
Rxd_0(P0.18)	-	Input / Output	Serial receiver I_0 / O_0
Txd_0(P0.19)	-	Output	Serial transmitter line 0

Table14.2 UART1 pins description

This buffer arrangement is sufficient for most simple embedded applications. For example, a processor running at 30MHz with a baud rate of 115200 means a character transfer every 30e6×(1+8+1)/115200=2604 cycles. For duplex communication, the processor might receive an interrupt every 1300 clock cycles. Because the interrupt response time and the handler execution time are usually quite short, this leaves sufficient processing time for the thread.

The design includes a double flip-flop SYNChronization logic for the receive data input.

14.1.1 UART Data Register (Address: 0x40004000h, 0x40005000h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	data	data	data	data	data	data	data	data
R	data	data	data	data	data	data	data	data
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

Data Data value.
Read : Received data.
Write : Transmit data

14.1.2 UART State Register (Address: 0x40004004h, 0x40005004h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								
R					state	state	state	state
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

State UART state.
[3] : RX buffer overrun, write 1 to clear.
[2] : TX buffer overrun, write 1 to clear.
[1] : RX buffer full, read-only.
[0] : TX buffer full, read-only.

14.1.3 UART Control Register (Address: 0x40004008h, 0x40005008h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W			Ctrl	Ctrl	Ctrl	Ctrl	Ctrl	Ctrl
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

Ctrl UART ctrl.
[5] : RX overrun interrupt enable.
[4] : TX overrun interrupt enable.

[3] : RX interrupt enable.
[2] : TX interrupt enable.
[1] : RX enable.
[0] : TX enable.

14.1.4 UART Interrupt State Register (Address: 0x4000400Ch, 0x4000500Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W					INTCLEAR	INTCLEAR	INTCLEAR	INTCLEAR
R					INTSTATE	INTSTATE	INTSTATE	INTSTATE
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

INTSTATE UART interrupt.
[3] : RX overrun interrupt. Write 1 to clear.
[2] : TX overrun interrupt. Write 1 to clear.
[1] : RX interrupt. Write 1 to clear.
[0] : TX interrupt. Write 1 to clear.

INTCLEAR UART interrupt clear when write 1 to correspond to the INTSTATE

14.1.5 UART Baud Divider Register (Address: 0x40004010h, 0x40005010h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	BaudDiv	BaudDiv	BaudDiv	BaudDiv	BaudDiv	BaudDiv	BaudDiv	BaudDiv
R	BaudDiv	BaudDiv	BaudDiv	BaudDiv	BaudDiv	BaudDiv	BaudDiv	BaudDiv
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	BaudDiv	BaudDiv	BaudDiv	BaudDiv	BaudDiv	BaudDiv	BaudDiv	BaudDiv
R	BaudDiv	BaudDiv	BaudDiv	BaudDiv	BaudDiv	BaudDiv	BaudDiv	BaudDiv
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W					BaudDiv	BaudDiv	BaudDiv	BaudDiv
R					BaudDiv	BaudDiv	BaudDiv	BaudDiv
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

BaudDiv Baud rate divider. The minimum number is 16.

15. IIC interface

A8137M0's I²C peripheral provides two-wire interface between the device and I²C -compatible device by the two-wire I²C serial bus. The I²C peripheral supports the following functions.

- Conforms to v2.1 of the I²C specification (published by Philips Semiconductor)
- Master transmitter / receiver
- Slave transmitter / receiver
- Flexible transmission speed MODEs: Standard (up to 100 Kb/s) and Fast (up to 400Kb/s)
- Multi-master systems supported
- Supports 7-bit addressing MODEs on the I²C bus
- Interrupt generation
- Allows operation from a wide range of input clock frequencies (build-in 8-bit timer)

PIN 25 and PIN 26 are I²C Interface in A8137M0. The alternate function is Port 0.4 and Port 0.5. User can set Altfuncset (0x40010018H) to set up the PIN function. Please refer the Chapter 11 for more detail information.

PIN	TYPE	DESCRIPTION
SCL(P0.4)	INPUT /OUTPUT	I²C clock input /output
SDA(P0.5)	INPUT/ OUTPUT	I²C data input /output

Table15.1 I²C interface pins description.

15.1 Master MODE I²C

The I²C master MODE provides an interface between a microprocessor and an I²C bus. It can be programmed to operate with arbitration and clock SYNChronization to allow it to operate in multi-master systems. Master MODE I²C supports transmission speeds up to 400Kb/s.

15.1.1 I²C REGISTERS

There are six registers used to interface to the host: the Control, Status, Slave Address, Transmitted Data, Received Data and Timer Period Register.

Register	Address
Slave address – I²CMSA	0x50003000
Control – I²CMCR	0x50003004
Transmitted data I²CBUF	0x50003008
Timer period - I²CMTP	0x5000300C
SCL low time-SCL_LP	0x50003010
SCL high time-SCL_HP	0x50003014
SDA setup time-SDA_SU	0x50003018
Interrupt – I²CMINT	0x5000301C

Table15.2 I²C Registers for writing.

Register	Address
Slave address – I²CMSA	0x50003000
Status – I²CMSR	0x50003004
Received data - I²CBUF	0x50003008
Timer period - I²CMTP	0x5000300C
SCL low time-SCL_LP	0x50003010
SCL high time-SCL_HP	0x50003014
SDA setup time-SDA_SU	0x50003018
Interrupt – I²CMINT	0x5000301C

Table15.3 I²C Registers for reading.

■ **I²C Master MODE Timer Period Register**

To generate wide range of SCL frequencies the core have built-in 8-bit timer. Programming sequence must be done at least once after system reset. After reset, register have 0x01 value by default.

SCL_PERIOD = 2 x (1+TIMER_PRD) x (SCL_LP + SCL_HP) x CLK_PRD
For example： - CLK_PRD = 62.5ns (CLK_FRQ = 16MHz)；

- TIMER_PRD =3； - SCL_LP = 6；(fixed) - SCL_HP = 4; (fixed)
SCL_PERIOD = 2 x (1 + 3) x (6 + 4) x 62.5ns = 5000ns = 5us
SCL_FREQUENCY = 1 / 5us = 200 KHz
SCL_PRD - SCL line period (I^2C clock line)
TIMER PRD -Timer period register value (range 1 to 255)
CLK_PRD - System clock period ($1/f_{clk}$)

15.1.2 I^2C Timer Period Register (Address: 0x5000300Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	P.6	P.5	P.4	P.3	P.2	P.1	P.0	P.6
R	P.6	P.5	P.4	P.3	P.2	P.1	P.0	P.6
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

■ I^2C CONTROL AND STATUS REGISTERS

The Control Register consists of eight bits: the RUN, START, STOP, ACK, HS, ADDR, SLRST and RSTB bit. The RSTB bit performs reset of whole I^2C controller and behaves identically as external reset provided by RST pin. Using this bit software application can reinitialize I^2C mater module when some problem is encountered on I^2C bus. In case when I^2C Slave device bloCKS I^2C bus, then SLRST bit should be set along with RUN bit (just after issuing the RSTB). SLRST bit causes that I^2C master module generates 9 SCK cloCKS (no START is generated) to recover Slave device to known state and issues at the end STOP. This bit is automatically cleared by I^2C MASTER MODULE, thus, it is always read as '0'. The BUSY bit should be checked to know when this transmission is ended.

The START bit will cause the generation of the START, or REPEATED START condition. The STOP bit determines if the cycle will stop at the end of the data cycle, or continue on to a burst. To generate a single send cycle, the Slave Address register is written with the desired address, the R/S bit is set to '0', and Control Register is written with HS=0, ACK=x, STOP=1, START=1, RUN=1 (binary xxx0x111 x-mean 0 or 1) to perform the operation and stop. When the operation is completed (or aborted due an error), the interrupt is generated. The data may be read from Received Data Register. When I^2C MASTER MODULE core operates in Master receiver MODE the ACK bit must be set normally to logic 1. This cause the I^2C MASTER MODULE bus controller to send acknowledge automatically after each byte. This bit must be reset when the I^2C MASTER MODULE bus controller requires no fuRTHer data to be sent from slave transmitter.

The ADDR bit along with RUN bit cause the generation of the START condition and transmission of Slave Address. Next STOP can end transmission, or REPEATED START generates the START and ADDRRESS sequence once again. In both cases STOP can ends transmission. See I^2C MASTER MODULE ACK Polling chapter for details.

15.1.3 I^2C Control Register (Address: 0x50003004h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RSTB	SLRST	ADDR	HS	ACK	STOP	START	RUN
R	RSTB	SLRST	ADDR	HS	ACK	STOP	START	RUN
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-

R	-	-	-	-	-	-	-	-

RSTB	SLRST	ADDR	HS	R/S	ACK	STOP	START	RUN	OPERATION
0	0	0	0	0	-	0	1	1	START condition followed by SEND (Master remains in Transmitter MODE)
0	0	0	0	0	-	1	1	1	START condition followed by SEND and STOP condition
0	0	0	0	1	0	0	1	1	START condition followed by RECEIVE operation with **negative Acknowledge** (Master remains in Receiver MODE)
0	0	0	0	1	0	1	1	1	START condition followed by RECEIVE and STOP condition
0	0	0	0	1	1	0	1	1	START condition followed by RECEIVE (Master remains in Receiver MODE)
0	0	0	0	1	1	1	1	1	**forbidden sequence**
0	0	0	1	0	0	0	0	1	Master Code sending and switching to High-speed MODE
1	0	0	-	-	-	-	-	-	I^2CM module software reset
0	1	0	0	0	0	0	0	1	Reset slaves connected to I^2C bus by generating 9 SCK cloCKS followed by STOP
0	0	1	0	0	0	0	0	1	START condition followed by Slave Address

Table14.5 Control bits combinations permitted in IDLE state *

RSTB	SLRST	ADDR	HS	R/S	ACK	STOP	START	RUN	OPERATION
0	0	0	0	-	-	0	0	1	SEND operation (Master remains in Transmitter MODE)
0	0	0	0	-	-	1	0	0	STOP condition
0	0	0	0	-	-	1	0	1	SEND followed by STOP condition
0	0	0	0	0	-	0	1	1	Repeated START condition followed by SEND (Master remains in Transmitter MODE)
0	0	0	0	0	-	1	1	1	Repeated START condition followed by SEND and STOP condition
0	0	0	0	1	0	0	1	1	Repeated START condition followed by RECEIVE operation with **negative Acknowledge** (Master remains in Receiver MODE)
0	0	0	0	1	0	1	1	1	Repeated START condition followed by SEND and STOP condition
0	0	0	0	1	1	0	1	1	Repeated START condition followed by RECEIVE (Master remains in Receiver MODE)
0	0	0	0	1	1	1	1	1	**forbidden sequence**
1	0	0	-	-	-	-	-	-	I^2CM module software reset
0	0	1	0	0	-	0	1	1	Repeated START condition followed by Slave Address

Table14.6 Control bits combinations permitted in Master Transmitter MODE

RSTB	SLRST	ADDR	HS	R/S	ACK	STOP	START	RUN	OPERATION
0	0	0	0	-	0	0	0	1	RECEIVE operation with **negative Acknowledge** (Master remains in Receiver MODE)
0	0	0	0	-	-	1	0	0	STOP condition**
0	0	0	0	-	0	1	0	1	RECEIVE followed by STOP condition
0	0	0	0	-	1	0	0	1	RECEIVE operation (Master remains in Receiver MODE)
0	0	0	0	-	1	1	0	1	**forbidden sequence**

0	0	0	0	1	0	0	1	1	Repeated START condition followed by RECEIVE operation with **negative Acknowledge** (Master remains in Receiver MODE)
0	0	0	0	1	0	1	1	1	Repeated START condition followed by RECEIVE and STOP condition
0	0	0	0	1	1	0	1	1	Repeated START condition followed by RECEIVE (Master remains in Receiver MODE)
0	0	0	0	0	-	0	1	1	Repeated START condition followed by SEND (Master remains in Transmitter MODE)
0	0	0	0	0	-	1	1	1	Repeated START condition followed by SEND and STOP condition
1	0	0	-	-	-	-	-	-	I^2CM module software reset

Table14.7 Control bits combinations permitted in Master Receiver MODE

The status Register is consisted of six bits：the BUSY bit, the ERROR bit, the ADDR_ACK bit, the DATA_ACK bit, the ARB_LOST bit, and the IDLE bit.

15.1.4 I^2C Control Register (Address: 0x50003004h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	-	BUS_BUSY	IDLE	ARB_LOST	DATA_ACK	ADDR_ACK	ERROR	BUSY
R	-	BUS_BUSY	IDLE	ARB_LOST	DATA_ACK	ADDR_ACK	ERROR	BUSY
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

IDLE：This bit indicates that I^2C BUS controller is in the IDLE state。
BUSY：This bit indicates that I^2C BUS controller receiving, or transmitting data on the bus, and other bits of Status register are no valid;
BUS_BUSY：This bit indicates that the Bus is Busy, and access is not possible. This bit is set / reset by START and STOP conditions;
ERROR：This bit indicates that due the last operation an error occurred: slave address wasn't acknowledged, transmitted data wasn't acknowledged, or I^2C Bus controller lost the arbitration;
ADDR_ACK：This bit indicates that due the last operation slave address wasn't acknowledged;
ARB_LOST：This bit indicates that due the last operation I^2C Bus controller lost the arbitration;

■ **SLAVE ADDRESS REGISTER**

The Slave address Register consists of eight bits：Seven address bits (A6-A0), and Receive/ not send bit R/S. The R/S bit determines if the next operation will be a Receive (high), or Send (low).

15.1.5 I^2C Slave Address Register (Address: 0x50003000h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	A.6	A.5	A.4	A.3	A.2	A.1	A.0	R/S
R	A.6	A.5	A.4	A.3	A.2	A.1	A.0	R/S
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								

R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

■ **I²C Data Buffer – RECEIVER AND TRANSMITTER REGISTERS**

I²C module has two separated 1 byte buffer in receiver and transmitter and these are located in the same address (0xF6). The Transmitted Data Register consists of eight data bits which will be sent on the bus due the next Send, or Burst Send operation. The first send bit is D.7 (MSB).

15.1.6 I²C Data Register (Address: 0x50003008h)

R/W	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
W	D.7	D.6	D.5	D.4	D.3	D.2	D.1	D.P
R	D.7	D.6	D.5	D.4	D.3	D.2	D.1	D.P
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

The Receiver Data Register consists of eight data bits which have been received on the bus due the last receive, or Burst Receive operation.

15.1.7 I²C Data Register (Address: 0x50003008h)

R/W	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
W	D.7	D.6	D.5	D.4	D.3	D.2	D.1	D.P
R	D.7	D.6	D.5	D.4	D.3	D.2	D.1	D.P
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

15.1.8 I²C MASTER MODULE AVAILABLE SPEED MODES

Default transmission parameter/constant values are shown in sections below. SCL clock frequency can be changed by modification of timer period values as show in the table below.

■ **I²C MASTER MODULE STANDARD MODE**

Typical configuration values for Standard speed MODE：

The following table gives an example parameters for standard I²C speed MODE.

System clock	TIMER_PERIOD	Transmission speed
4 MHz	1 (01h)	100kb/s
6 MHz	2 (02h)	100kb/s
10 MHz	4 (04h)	100kb/s
16 MHz	7 (07h)	100kb/s
20 MHz	9 (09h)	100kb/s

Table15.4 I²C MASTER MODULE Timer period values for standard speed MODE.

■ **I²C MASTER MODULE FAST MODE**

Typical configuration values for Fast speed MODE：

The following table gives example parameters for Fast I²C speed MODE.

System clock	TIMER_PERIOD	Transmission speed
10 MHz	1 (01h)	250 Kb/s
16 MHz	1 (01h)	400 Kb/s
20 MHz	2 (02h)	333 Kb/s

Table15.5 I²C MASTER MODULE Timer period values for Fast speed MODE.

15.1.9 I²C MASTER MODULE AVAILABLE COMMAND SEQUENCES

■ **I²C MASTER MODULE SINGLE SEND**

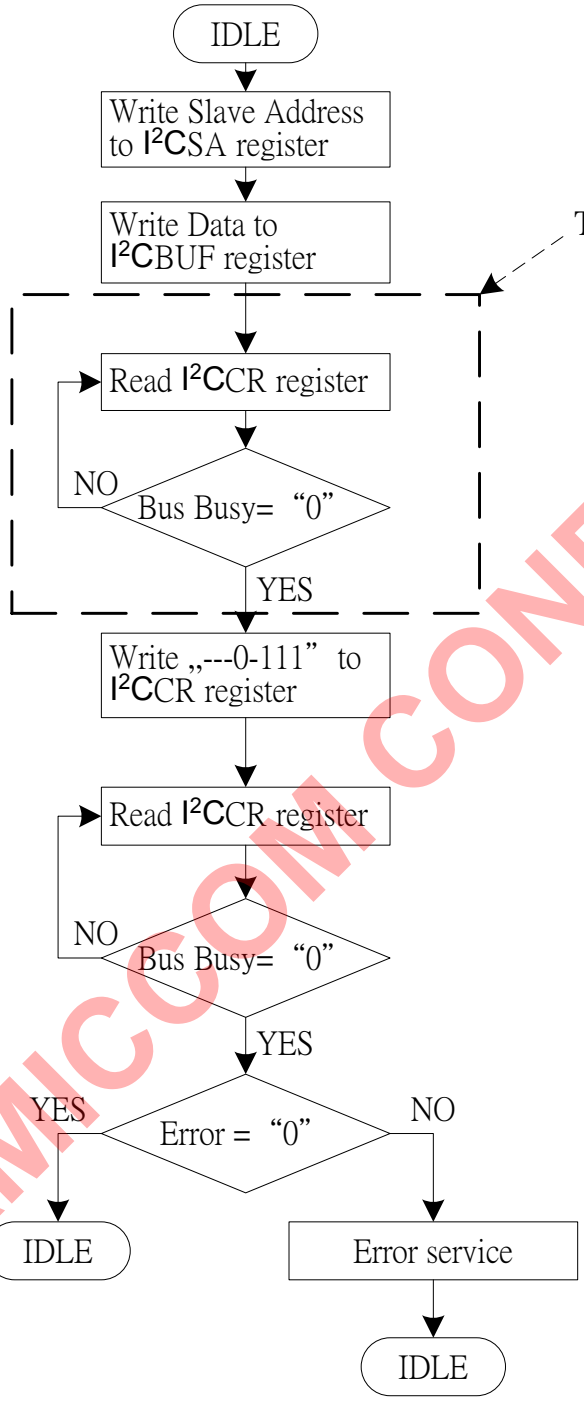


Figure15.1 I²C MASTER MODULE Single SEND flowchart

■ I²C MASTER MODULE SINGLE RECEIVE

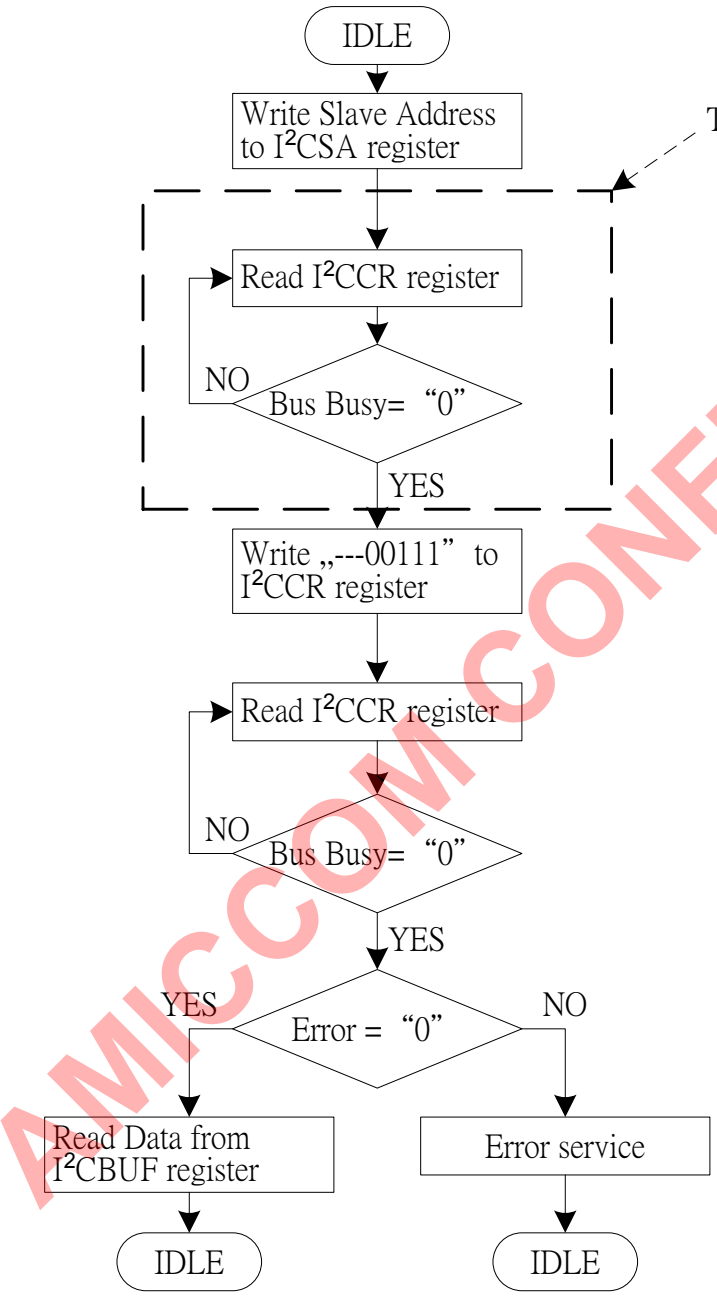


Figure15.2 Single RECEIVE flowchart

■ I²C MASTER MODULE BURST SEND

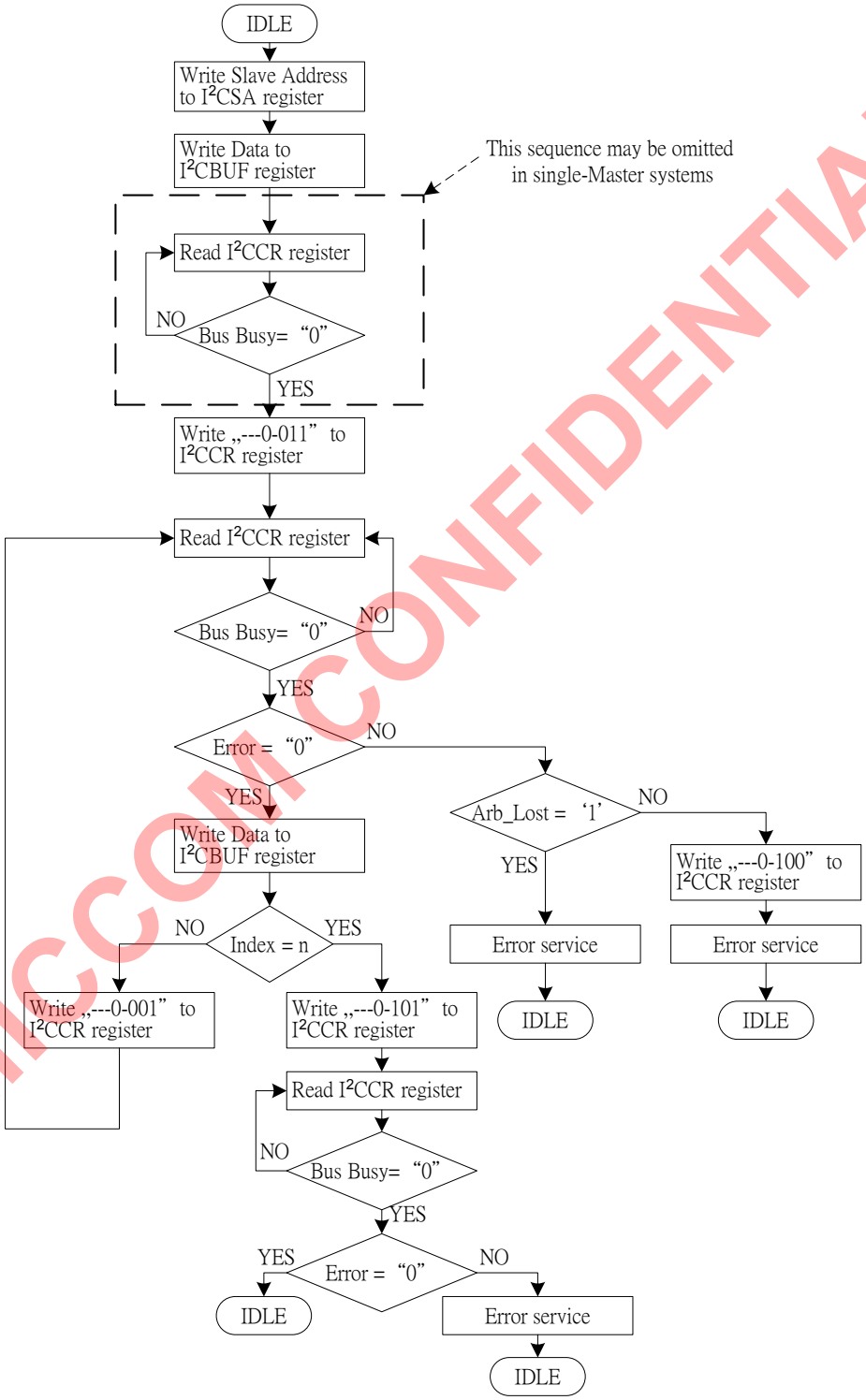


Figure15.3 I²C MASTER MODULE Sending n bytes flowchart

■ I²C MASTER MODULE BURST RECEIVE

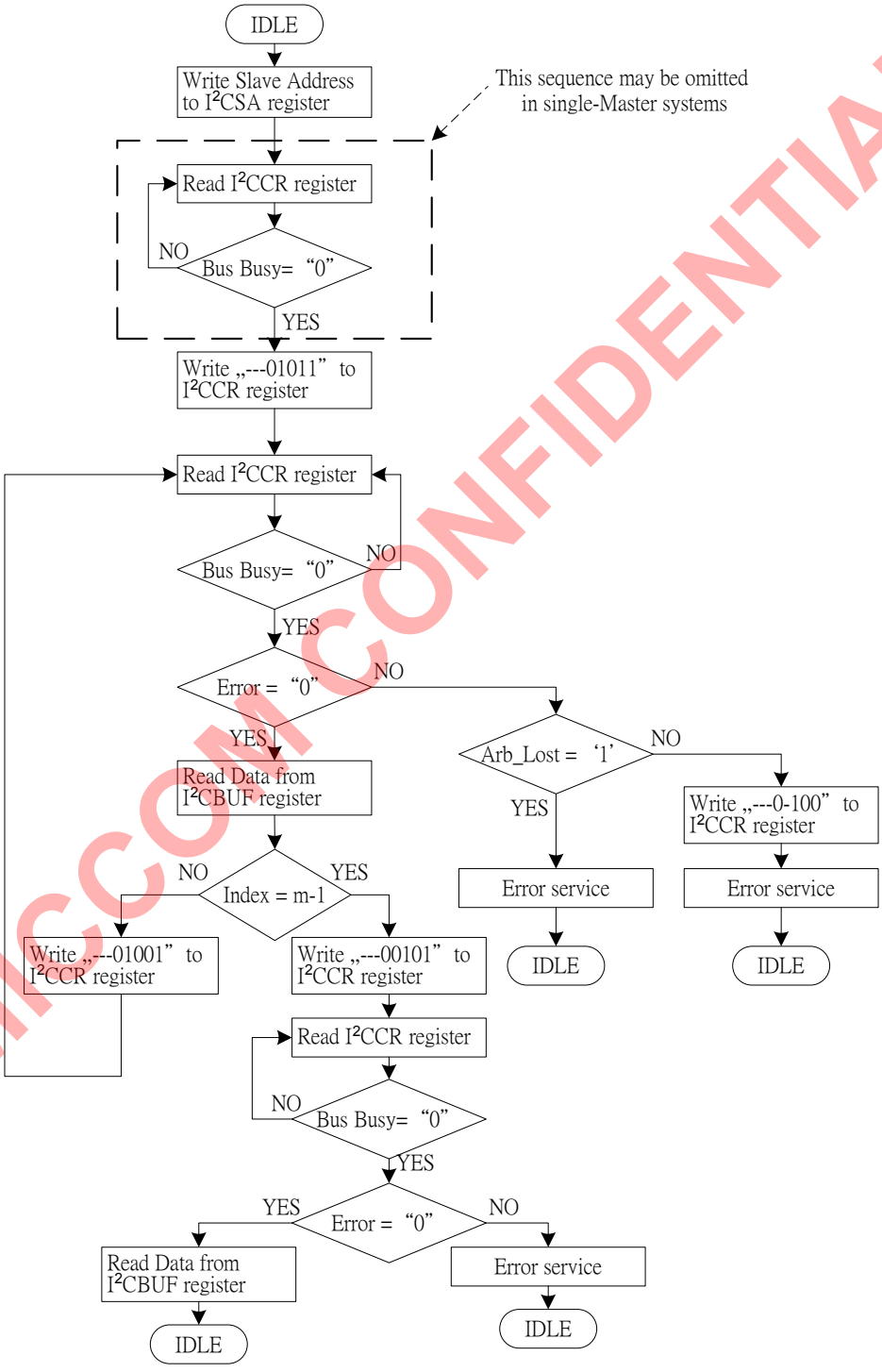


Figure15.4 I²C MASTER MODULE Receiving m bytes flowchart

■ I²C MASTER MODULE BURST RECEIVE AFTER BURST SEND

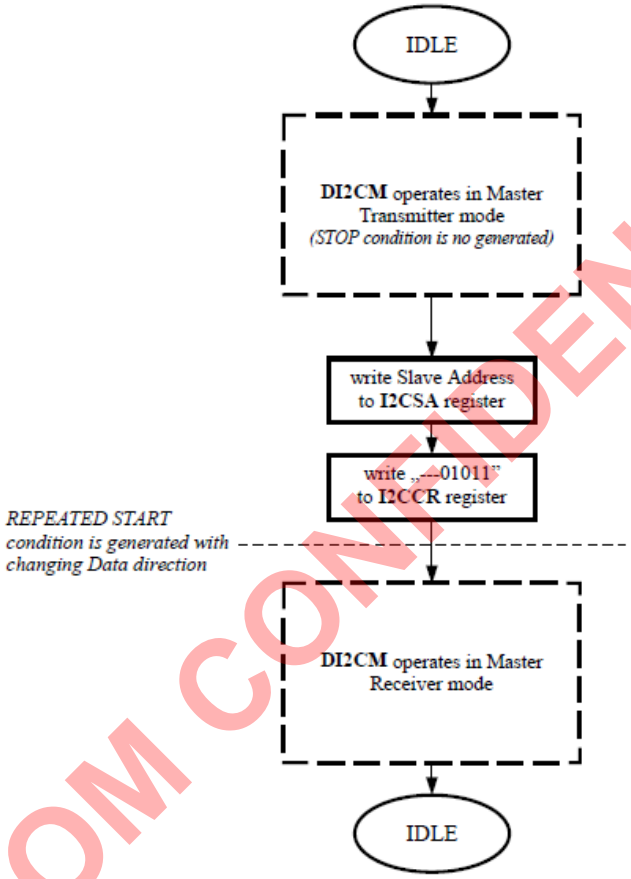


Figure15.5 I²C MASTER MODULE Sending n bytes then Repeated Start and Receiving m bytes flowchart

■ **I²C MASTER MODULE BURST SEND AFTER BURST RECEIVE**

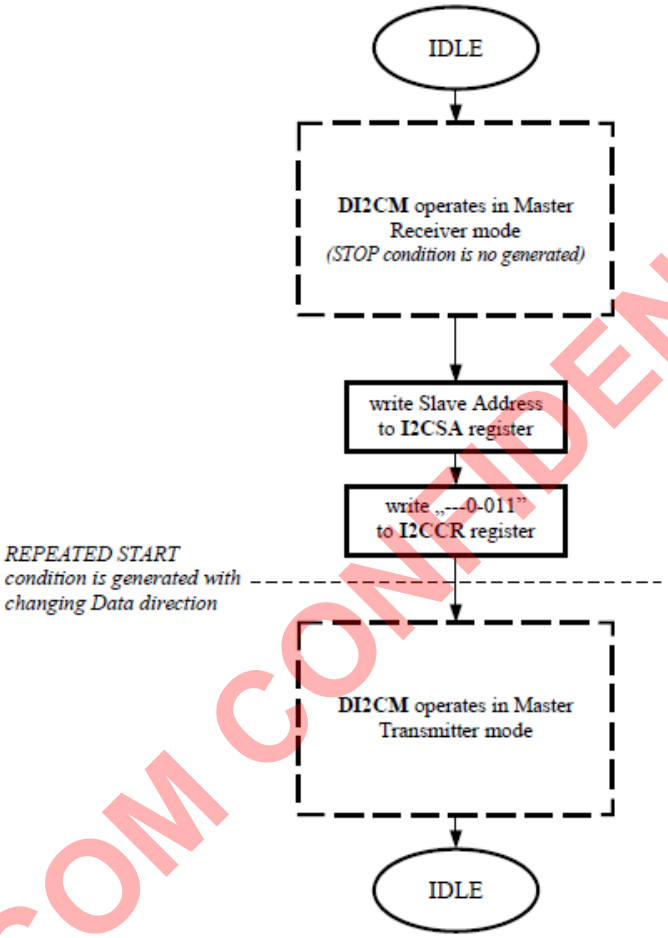


Figure15.6 I²C MASTER MODULE Receiving m bytes then Repeated Start and Sending n bytes flowchart

■ **I²C MASTER MODULE ACK POLLING**

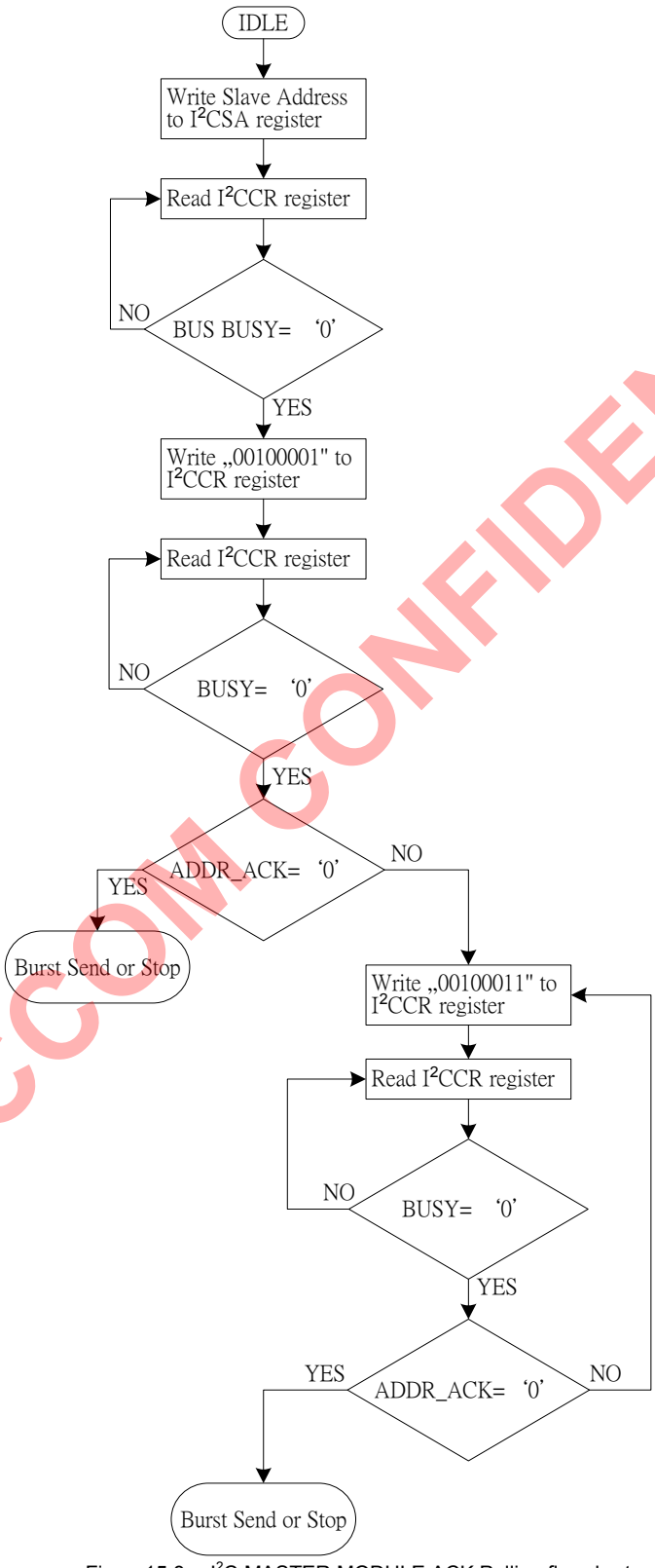


Figure15.8 I²C MASTER MODULE ACK Polling flowchart

15.2 I²C MASTER MODULE INTERRUPT GENERATION

I²C MASTER MODULE interrupt flag is automatically asserted when I²C transfer (send or receive a byte) is completed or transfer error has occurred. I²CMIF flag has to be cleared by software.

Interrupt flag	Function
I²CMIF	Internal, I²C MASTER MODULE

Table15.6 I²C MASTER MODULE interrupt summary

15.2.1 I²C Master Interrupt Register (Address: 0x5000301Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W							I²CMIF	I²CMIE
R							I²CMIF	I²CMIE
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

I²CMIF：I²C MASTER MODULE interrupt flag

It must be cleared by software writing logic '1'. Writing '0' does not change its content.

I²CMIE：I²C MASTER MODULE interrupt enable

Please refer the Chapter 10.3.2 for more detail information.

15.3 Slave MODE I²C

The I²C module provides an interface between a microprocessor and I²C bus. It can works as a slave receiver or transmitter depending on working MODE determined by microprocessor/microcontroller. The core incorporates all features required by I²C specification. The I²C module supports all the transmission MODEs: Standard and Fast.

15.3.1 I²C MODULE INTERNAL REGISTERS

There are five registers used to interface to the target device：The Own Address, Control, Status, Transmitted Data and Received Data registers.

Register	Address
Own address – I²CSOA	0x50003804
Control – I²CSCR	0x50003808
Transmitted data – I²CSBUF	0x5000380C
Own address up– I²CSOAUP	0x50003810
Interrupt – I²CSINT	0x50003014

Table15.7 I²C MODULE Registers for writing

Register	Address
Own address – I²CSOA	0x50003804
Control – I²CSSR	0x50003808
Received data – I²CSBUF	0x5000380C
Own address up– I²CSOAUP	0x50003810
Interrupt – I²CSINT	0x50003814

Table15.8 I²C MODULE Registers for reading

■ **I²CSOA – OWN ADDRESS REGISTER**

The Own Address Register consists of seven address bits which identify I²C module core on I²C Bus. This register can be read and written at the address 0xF1.

15.3.2 I²C Own Address Register (Address: 0x50003804h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W		A.6	A.5	A.4	A.3	A.2	A.1	A0
R		A.6	A.5	A.4	A.3	A.2	A.1	A0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

■ **I²CSCR – CONTROL AND STATUS REGISTERS**

The Control Register consists of the bits：The RSTB and DA bit. The RSTB bit performs reset of whole I²C controller and behaves identically as external reset provided by RST pin. Using this bit software application can reinitialize I²C module when some problem is encountered on I²C bus. The DA bit enables (‘1’) and disable (‘0’) the I²C module device operation. DA is set immediately to ‘1’ when MCU write DA=1. This register can be only written at address 0xF2. Reading this address puts status register on data bus – see below.

15.3.3 I²C Slave Control Register (Address: 0x50003808h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RSTB	DA	-	-	RECFINCLR	SENDFINCLR	-	-
R	RSTB	DA	-	-	RECFINCLR	SENDFINCLR	-	-
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

DA：Device Active – enable or disable the I²C module device operation;
RSTB：Reset of whole I²C controller by writing ‘1’ to this bit. It behaves identically as RST pin
RECFINCLR：Writing ‘1’ to this bit clears RECFIN bit from the I²C MODULE status register.
SENDFINCLR：Writing ‘1’ to this bit clears SENDFIN bit from the I²C MODULE status register.

The Status Register consists of five bits: the DA, BUSACTIVE, RECFIN, SENDFIN bit, RREQ bit, TREQ bit. The receive finished RECFIN bit indicates that Master I²C controller has finished transmitting of data during single or burst receive operations. It also causes generation of interrupt on IRQ pin. The send finished SENDFIN bit indicates that Master I²C controller has finished receiving of data during single or burst send operations. It also causes generation of interrupt on IRQ pin. The Receive Request RREQ bit indicates that I²C module device has received data byte from I²C master. I²C module host device (usually MCU) should read one data byte from the Received Data register I²CSBUF. The Transmit Request TREQ bit indicates that I²C MODULE device is addressed as Slave Transmitter and I²C module host device (usually MCU) should write one data byte into the Transmitted Data register I²CSBUF. The BUSACTIVE ‘1’ signalizes that any transmission (send, receive or own address detection) is in progress. BUSACTIVE is cleared (‘0’) automatically by I²C module in case when there is no any transmission. This is read only bit.

The DA bit should be polled (read) when MCU wrote DA=0. The DA bit is not immediately cleared when any I²C transmission (send, receive or own address detection) is in progress. When current transmission has completed then this bit is cleared to ‘0’ and I²C module become inactive.

15.3.4 I²C Slave State Register (Address: 0x50003808h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W		DA	-	BUSACTIVE	RECFIN	SENDFIN	TREQ	RREQ
R		DA	-	BUSACTIVE	RECFIN	SENDFIN	TREQ	RREQ
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

DA：Device Active – enable (‘1’) or disable (‘0’) the I²C MODULE device operation;
BUSACTIVE：Bus ACTIVE – ‘1’ signalizes that any transmission: send, receive or own address detection is in progress;
RREQ：Indicates that I²C module device has received data byte from I²C master;
It is automatically cleared by read of I²CSBUF.
TREQ：Indicates that I²C module device is addressed as transmitter and requires data byte from host device;
It is automatically cleared by write data I²CSBUF.
RECFIN：Indicates that Master I²C controller has ended transmit operation. It means that no more RREQ will be set during this single or burst I²C module receive operation. It is cleared by writing ‘1’ to the RECFINCLR bit in the I²C module control register.
SENDFIN：Indicates that Master I²C controller has ended receive operation. It means that no more TREQ will be set during this single or burst I²C module send operation. It is cleared by writing ‘1’ to the SENDFINCLR bit in the I²C control register.
NOTE：All bits are active at HIGH level (‘1’).

■ **I²CSBUF – RECEIVER AND TRANSMITTER REGISTERS**

The Transmitter Data Register consists of eight Data bits which will be sent on the bus due the next Send operation. The first send bit is the D.7(MSB).

15.3.5 I²C Data Register (Address: 0x5000380Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	D.7	D.6	D.5	D.4	D.3	D.2	D.1	D.P
R	D.7	D.6	D.5	D.4	D.3	D.2	D.1	D.P
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

The Receiver Data Register consists of eight data bits which have been received on the bus due the last Receive operation.

15.3.6 I²C Data Register (Address: 0x5000380Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	D.7	D.6	D.5	D.4	D.3	D.2	D.1	D.P
R	D.7	D.6	D.5	D.4	D.3	D.2	D.1	D.P
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**

W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

15.4 AVAILABLE I²C MODULE TRANSMISSION MODES

This chapter describes all available transmission MODEs of the I²C module core. Default I²C own address for all presented waveforms is 0x39 ("0111001").

15.4.1 I²C module SINGLE RECEIVE

The figure below shows a set of sequences during Single data Receive by I²C MODULE. Single receive sequences：

- ✧ Start condition
- ✧ I²C module is addressed by I²C Master as receiver
- ✧ Address is acknowledged by I²C module
- ✧ Data is received by I²C module
- ✧ Data is acknowledged by I²C module
- ✧ Stop condition

15.4.2 I²C module SINGLE SEND

The figure below shows a set of sequences during Single data Send by I²C MODULE. Single send sequences：

- ✧ Start condition
- ✧ I²C module is addressed by I²C Master as transmitter
- ✧ Address is acknowledged by I²C module
- ✧ Data is transmitted by I²C module
- ✧ Data is not acknowledged by I²C Master
- ✧ Stop condition

15.4.3 I²C module BURST RECEIVE

The figure below shows a set of sequences during Burst data Receive by I²C module. Burst receive sequences：

- ✧ Start condition
- ✧ I²C module is addressed by I²C Master as receiver
- ✧ Address is acknowledged by I²C module
- ✧ (1)Data is received by I²C module
- ✧ (2)Data is acknowledged by I²C module
- ✧ STOP condition

Sequences (1) and (2) are repeated until Stop condition occurs.

15.4.4 I²C module BURST SEND

The figure below shows a set of sequences during Burst Data Send by I²C module. Burst send sequences：

- ✧ Start condition
- ✧ I²C module is addressed by I²C Master as transmitter
- ✧ Address is acknowledged by I²C module
- ✧ (1)Data is transmitted by I²C module
- ✧ (2)Data is acknowledged by I²C Master
- ✧ (3)Last data is not acknowledged by I²C Master
- ✧ Stop condition

Sequences (1) and (2) are repeated until last transmitted data is not acknowledged (3) by I²C Master.

15.4.5 AVAILABLE I²C module COMMAND SEQUENCES FLOWCHART

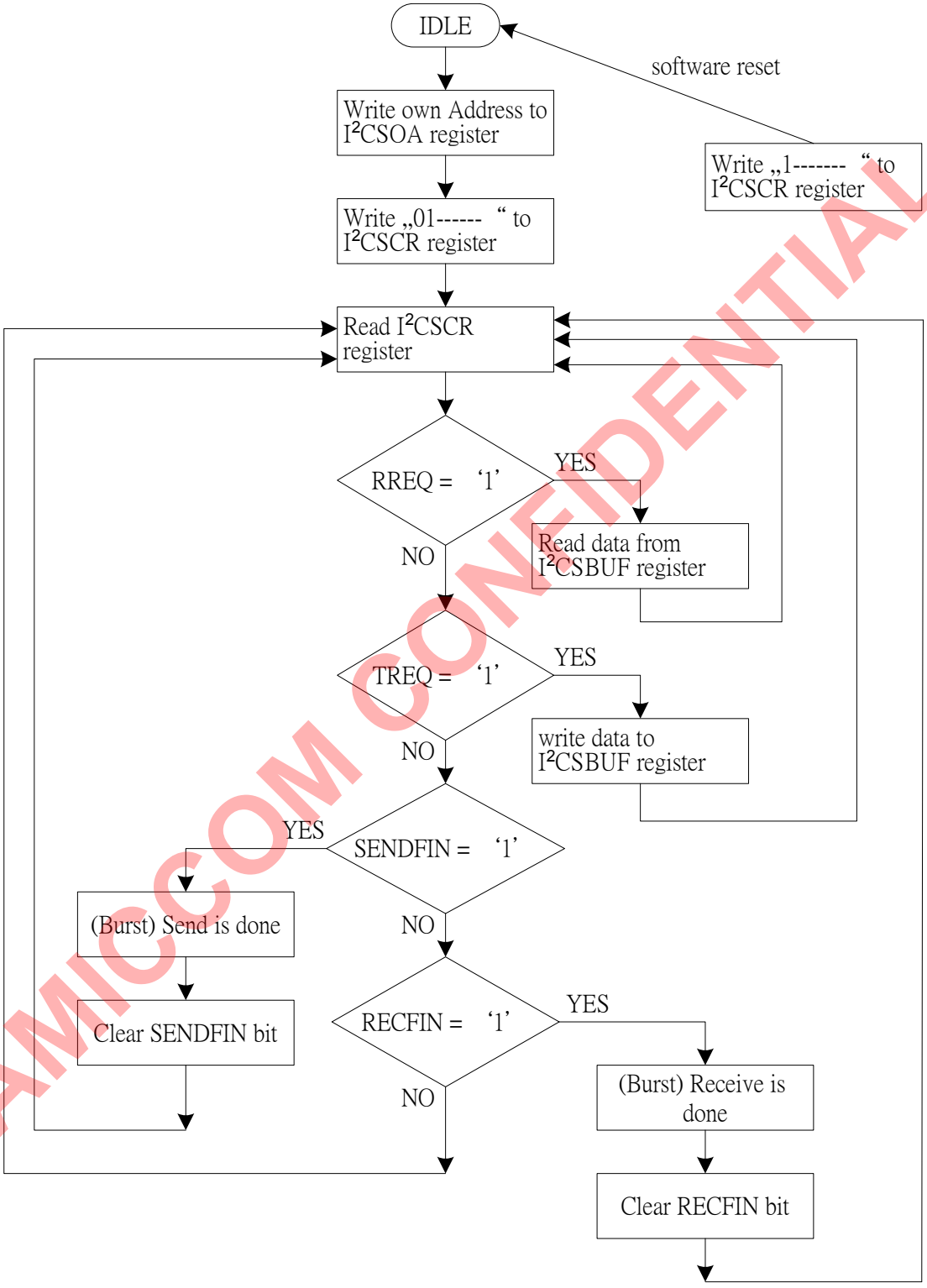


Figure15.9 Available I²C MODULE command sequences flowchart

15.5 I²C MODULE INTERRUPT GENERATION

I²C MODULE interrupt flag is automatically asserted when I²C transfer (send or receive a byte) is completed or transfer error has occurred. I²CSIF flag has to be cleared by software.

Interrupt flag	Function
I²CSIF	Internal, DI²CS

Table15.9 I²C MODULE interrupt summary

I²C MODULE related interrupt bits have been summarized below. The IE (0xA8) contains global interrupt system disable (0) / enable (1) bit called EA.

15.5.1 I²C Slave Interrupt Register (Address: 0x5000381Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W							I²CSIF	I²CSIE
R							I²CSIF	I²CSIE
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	-	-	-	-	-	-	-	-
R	-	-	-	-	-	-	-	-

I²CSIF：I²C MODULE interrupt flag

Software should determine the source of interrupt by check both modules' interrupt related bits. It must be cleared by software writing 0x80. It cannot be set by software.

I²CSIE：I²C MODULE interrupt enable

16. SPI interface

The SPI is a fully configurable SPI master/slave device, which allows user to configure polarity and phase of serial clock signal SCK.

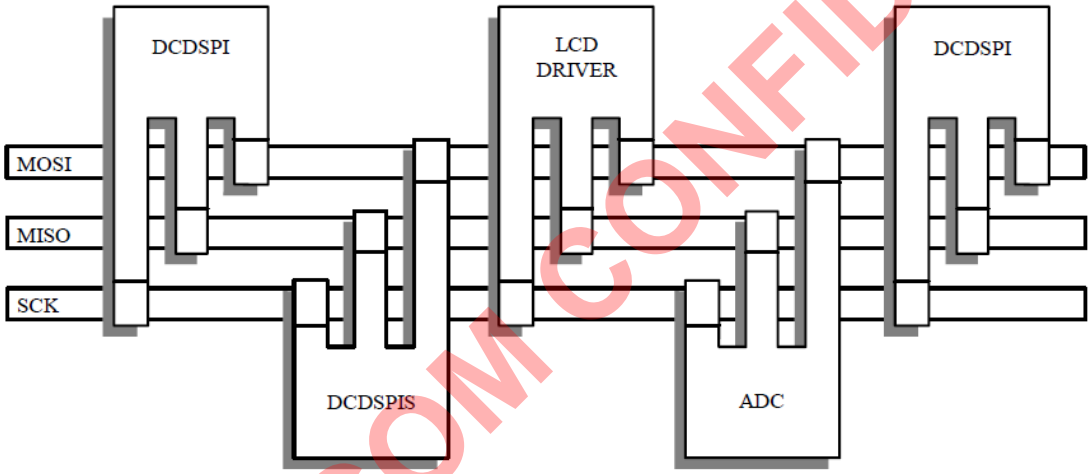
The SPI allows the microcontroller to communicate with serial peripheral devices. It is also capable of inter-processor communications in a multi-master system. A serial clock line (SCK) SYNChronizes shifting and sampling of the information on the two independent serial data lines. SPI data are simultaneously transmitted and received.

The SPI is a technology independent design that can be implemented in a variety of process technologies.

The SPI system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. The system can be configured as a master or a slave device. Data rates as high as System clock divided by four (CLK/4). Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols to accommodate most available SYNChronous serial peripheral devices. When the SPI is configured as a master, software selects one of four different bit rates for the serial clock.

The SPI automatically drive selected by SSCR (Slave Select Control Register) slave select output (SS0O), and address SPI slave device to exchange serially shifted data.

Error-detection logic is included to support inter-processor communications. A write-collision detector indicates when an attempt is made to write data to the serial shift register while a transfer is in progress. A multiple-master MODE-fault detector automatically disables SPI output drivers if more than one SPI devices simultaneously attempts to be become bus master.



16.1 KEY FEATURES

All features listed below are included in the current version of SPI core.

- SPI Master
  - Full duplex SYNChronous serial data transfer
  - Master operation
  - Multi-master system supported
  - Up to 8 SPI slaves can be addressed
  - System error detection
  - Interrupt generation
  - Supports speeds up to 1/4 up to system clock
  - Bit rates generated 1/4, 1/8, 1/32, 1/64, 1/128, 1/256 of system clock
  - Four transfer formats supported
  - Simple interface allows easy connection to microcontrollers
- SPI Slave
  - Full duplex SYNChronous serial data transfer
  - Slave operation
  - System error detection
  - Interrupt generation
  - Supports speeds up to 1/4 of system clock

- Simple interface allows easy connection to microcontrollers
- Four transfer formats supported

- Fully synthesizable, static SYNChronous design with no internal tri-states

16.2 SPI PINS DESCRIPTION

PIN	TYPE	ACTIVE	DESCRIPTION
Scki_Scko(P0.3)	INPUT / OUTPUT	-	SPI clock input / output
SIMO(P0.2)	INPUT / OUTPUT	-	Slave serial data input / Master serial data output
MISO(P0.1)	INPUT / OUTPUT	-	Master serial data input / Slave serial data output
SSO(P0.0)	OUTPUT	low	Slave select output

Table16.1 SPI pins description

16.3 SPI HARDWARE DESCRIPTION

16.3.1 BLOCK DIAGRAM

When an SPI transfer occurs, an 8-bit character is shifted out on data pin while a different 8-bit character is simultaneously shifted in a second data pin. Another way to view this transfer is that an 8-bit shift register in the master and another 8-bit shift register in the slave are connected as a circular 16-bit shift register. When a transfer occurs, this distributed shift register is shifted eight bit positions; thus, the characters in the master and slave are effectively exchanged.

The central element in the SPI system is the block containing the shift register and the read data buffer. The system is single buffered in the transmit direction and double buffered in the receive direction. This fact means new data for transmission cannot be written to the shifter until the previous transaction is complete; however, received data is transferred into a parallel read data buffer so the shifter is free to accept a second serial character. As long as the first character is read out of the read data buffer before the next serial character is ready to be transferred, no overrun condition will occur.

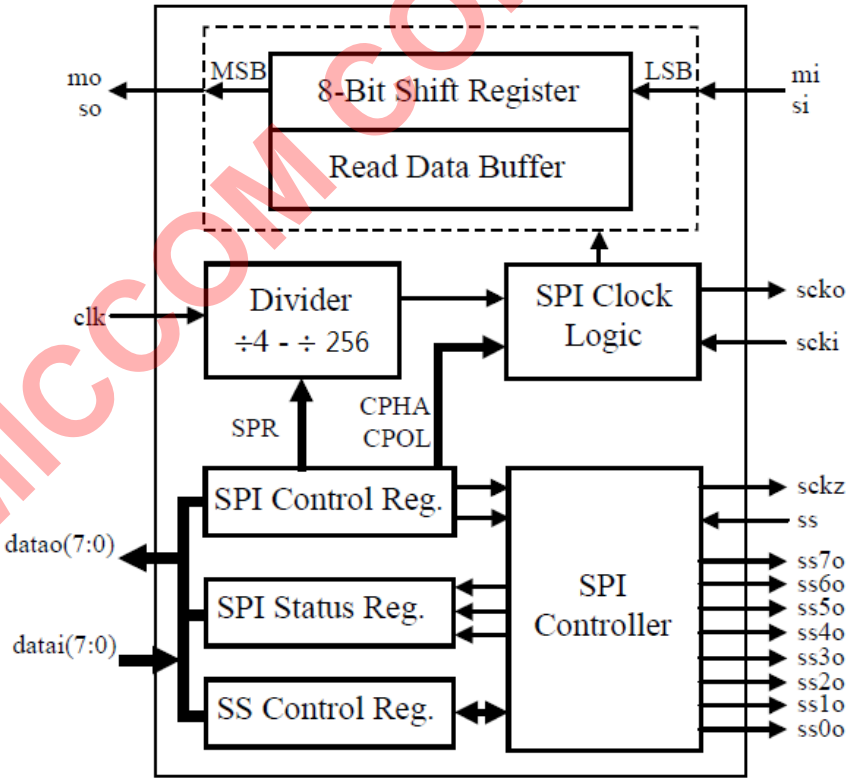


Figure 16.2 SPI Block Diagram

The eight pins are associated with the SPI: the SS, clock pins SCKI, SCKO and SCKEN, master pins MI and MO and slave pins SOEN, SI and SO.

The SS input pin in a master MODE is used to detect MODE-fault errors. A low on this pin indicates that some other device in a multi-master system has become a master and trying to select the SPI MODULE as a slave. The SS input pin in a slave MODE is used to enable transfer.

The SCKI pin is used when the SPI is configured as a slave. The input clock from a master SYNChronizes data transfer between a master and the slave devices. The slave device ignore the SCKI signal unless the SS (slave select) pin is active low.

The SCKO and SCKEN pins are used as the SPI clock signal reference in a master MODE. When the master initiates a transfer eight clock cycles is automatically generated on the SCKO pin.

When the SPI is configured as a slave the SI pin is the slave input data line, and the SO is the slave output data line.

When the SPI is configured as a master, the MI pin is the master input data line, and the MO is the master output data line.

16.3.2 INTERNAL REGISTERS

- **SPI Control Register**

The control register may be read or written at any time, is used to configure the SPI System.

- **SPI Control Register (Address: 0x50002000h)**

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	SPIE	SPE	SPR2	MSTR	CPOL	CPHA	SPR1	SPR0
R	SPIE	SPE	SPR2	MSTR	CPOL	CPHA	SPR1	SPR0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	Slave_TXFIFO_Reset			FIFOEN		bit_len	bit_len	bit_len
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W		rxfifo	rxfifo	rxfifo		txfifo	txfifo	txfifo
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

txfifo_il[2:0] : set TX FIFO interrupt level, if txfifo_il[2:0]>=txfifo_rem[2:0], generate interrupt
rxfifo_il[2:0] : set RX FIFO interrupt level, if rxfifo_il[2:0] <=rxfifo_rem[2:0], generate interrupt
fifoen：FIFO mode enable
In TX, We can write FIFOTXBUF continuously by software, the data is stored in FIFO, and the hardware starts to transfer data. when current data is finished, the next data starts to transfer automatically.
In RX, data is stored in FIFO by hardware, we can read FIFORXBUF many times by software.
= 0, SPI FIFO disable, SPI is the same as DCD SPI
= 1, SPI FIFO enable, FIFO is 8 depths * 16 bits
Slave_rst：wirte 1to clear slave TX FIFO
bit_len[3:0] : set number of bits in a shift sequence
= 0000~0011, 4 bits
= 0100, 5 bits
= 0101, 6 bits
= 0110, 7 bits
= 0111, 8 bits
= 1000, 9 bits
= 1001, 10 bits
= 1010, 11 bits
= 1011, 12 bits
= 1100, 13 bits
= 1101, 14 bits
= 1110, 15 bits
= 1111, 16 bits
SPIE：SPI interrupt enable
= 0, interrupts are disabled, polling MODE is used
= 1, interrupts are enabled
SPE：SPI system enable
= 0, system is off
= 1, system is on
MSTR：Master/Slave MODE select

= 0, slave
= 1, master

CPOL：Clock polarity select
= 0, high level; SCK idle low
= 1, low level; SCK idle high

CPHA：Clock phase.. Select one of two different transfer formats

SPR[2:0]：SPI clock rate select bits. See the table below

SPR2	SPR1	SPR0	System clock divided by
0	0	0	4
0	0	1	8
0	1	0	16
0	1	1	32
1	0	0	64
1	0	1	128
1	1	0	256
1	1	1	512

- **Slave Select Control Register**

The control register may be read or written at any time. It is used to configure which slave select output should be driven while SPI master transfer. Contents of SSCR register is automatically assigned on SS7O-SS0O pins when SPI master transmission starts.

■ **SPI Slave Control Register (Address: 0x5000200Ch)**

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								SS0
R								SS0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

SS0 Slave select control
= 0, Pin SSxO assigned while Master Transfer
= 1, Pin SSxO is forced to logic 1

■ **SPI Status Control Register (Address: 0x50002004h)**

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	SPIF	WCOL	-	MODF	-	-	-	SSCEN
R	SPIF	WCOL	-	MODF	-	-	-	SSCEN
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

SPIF：SPI interrupt request. The flag is automatically set to one at the end of an SPI transfer.
WCOL：Write collision error status flag. The flag is automatically set if the SPDR is written while a transfer is in process.
MODF：SPI MODE-fault error status flag

This flag is set if SS pin goes to active low while the SPI is configured as a master (MSTR = 1)

SSCEN：

= 1, auto SS assertions enabled

= 0, auto SS assertions disabled – SSO always shows contents of SSCR

SPI status register (SPSR) contains flags indicating the completion of transfer or occurrence of system errors. All flags are set automatically when the corresponding event occur and cleared by software sequence. SPIF and WCOL are automatically cleared by reading SPSR followed by an access of the SPDR. MODF flag is cleared by reading SPSR with MODF set followed by a write to SPCR.

The SSCSEN bit is a enable bit of automatic Slave Select Outputs assertion. When SSCEN is set ('1') then during master transmission the SSXO lines are automatically loaded with contents of SSCR register before each byte transfer, and deasserted when byte is transferred. When SSCEN bit is cleared the SSXO lines always shows contents of the SSCR register, regardless of the transmission is in progress or SPI MODULE is in IDLE state.

- Receiver and Transmitter Registers

The Transmitted Data Register consists of eight data bits, which will be sending on the bus due the next Send operation. The first send bit is the D.7 (MSB).

- **SPI TX FIFO Buffer Register (Address: 0x50002018h)**

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	data	data	data	data	data	data	data	data
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	data	data	data	data	data	data	data	data
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

The Received Data Register consists of eight data bits, which were received on the bus due the last Receive operation.

- **SPI RX FIFO Buffer Register (Address: 0x5000201Ch)**

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	data	data	data	data	data	data	data	data
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	data	data	data	data	data	data	data	data
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

16.4 MASTER OPERATIONS

When the SPI MODULE core is configured as a SPI master, the transfer is initiated by write to the SPDR register. When the new byte is written to the SPDR register, SPI MODULE begins transfer on the nearest BAUD timer overflow. The serial clock SCK is generated by the SPI MODULE. In master MODE the SPI MODULE activates the SCKEN to enable the SCK output driver.

The SPI MODULE in master MODE can select one of the eight SPI slave devices, through the SSxO lines. The SSxO lines – Slave Select output lines are loaded with contents of the SSCR register (0x03). The SSCEN bit from the SPSR register

select between automatic SSxO lines control and software control. When set the automatic Slave Select outputs assertion is enabled. With SSCEN bit set in master MODE the SSXO lines are automatically loaded with contents of SSCR register before each byte transfer, and deasserted when byte is transferred. When SSCEN bit is cleared the SSXO lines are controlled by the software, and always shows contents of the SSCR register, regardless of the transmission is in progress or the SPI MODULE is in IDLE state.

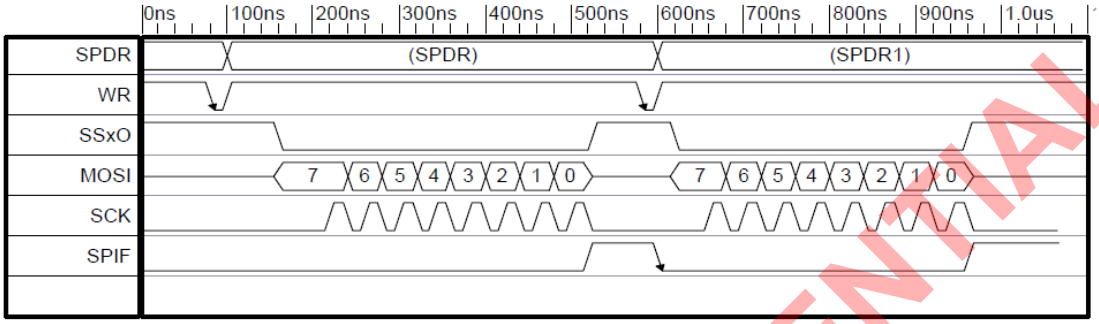


Figure16.3 Automatic slave select lines assertion

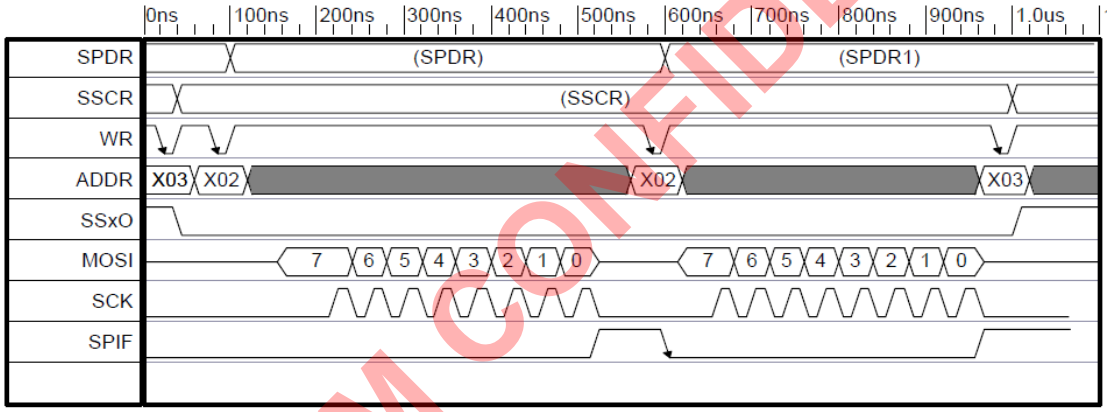


Figure16.4 Software controlled SSxO lines

16.4.1 MASTER MODE ERRORS

In master MODE two system errors can be detected by the SPI MODULE. The first type of error arises in multiple-master system when more than one SPI device simultaneously tries to be a master. This error is called a MODE Fault. The second error type, a Write Collision, indicates that MCU tried to write the SPDR register while transfer was in progress.

◆ **MODE FAULT ERROR**

MODE fault error occurs when the SPI MODULE is configured as a master and some other SPI master device will select this device as if it were a slave. If a MODE Fault Error occur：

- ✧ The MSTR bit is forced to zero to reconfigure the SPI MODULE as a slave.
- ✧ The SPE bit is forced to zero to disable the SPI MODULE system
- ✧ The MODF status flag is set and an interrupt request is generated

The MODF flag is cleared by reading SPSR with MODF set followed by a write to SPCR

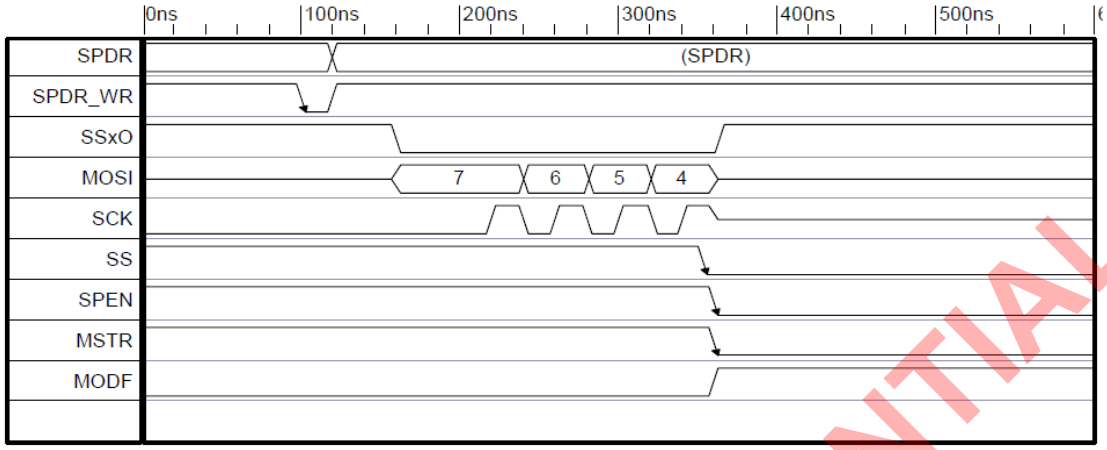


Figure16.5 MODE Fault Error generation

◆ **WRITE-COLLISION ERROR**

A write collision occurs if the SPI MODULE data register is written while a transfer is in progress. The transfer continues undisturbed, and the write data that caused the error is not written to the shifter. The Write Collision is indicated by the WCOL flag in SPSR (3) register.

The WCOL flag is set automatically by hardware, when the WCOL error condition occurs. To clear the WCOL bit, user should execute the following sequence:

- ✧ Read contents of the SPSR register
- ✧ Perform access to the SPDR register (read or write)

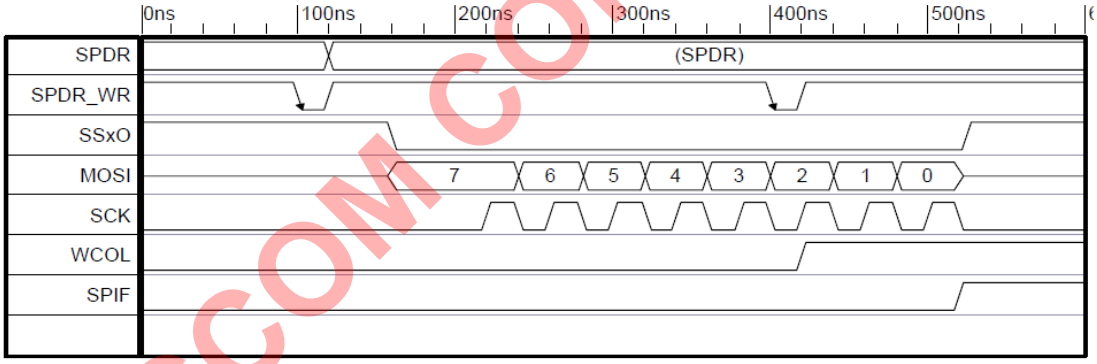


Figure16.6 Write Collision Error in SPI Master MODE

16.5 SLAVE OPERATIONS

When configured as SPI Slave the SPI MODULE transfer is initiated by external SPI master module by assertion of the SPI MODULE Slave Select input, and generation of the SCK serial clock.

Before transfer starts, the SPI master has to assert the Slave Select line to determine which SPI slave will be used to exchange data. The SS is asserted (cleared = 0), the clock signal connected to the SXCK line will cause the SPI MODULE slave to shift into receiver shift register contents of the MOSI line, and drives the MISO line with contents of the Transmitter Shift register. When all eight bits are shifted in/out the SPI MODULE generates the Interrupt request by setting the IRQ output.

In SPI MODULE slave MODE only one transfer error is possible – Write Collision Error.

16.5.1 SLAVE MODE ERRORS

In slave MODE, only the Write Collision Error can be detected by the SPI MODULE.

The Write Collision Error occurs when the SPDR register write is performed while the SPI MODULE transfer is in progress.

In SLAVE MODE when the CPHA is cleared, the write collision error may occur as long as the SS Slave Select line is driven low, even if all bits are already transferred. This is because there is not clearly specified the transfer beginning, and SS driven low after full byte transfer may indicate beginning of the next byte transfer.

◆ **WRITE-COLLISION ERROR**

A write collision occurs if the SPI MODULE data register is written while a transfer is in progress. The transfer continues undisturbed, and the write data that caused the error is not written to the shifter. The Write Collision is indicated by the WCOL flag in SPSR (3) register.

The WCOL flag is set automatically by hardware, when the WCOL error condition occurs. To clear the WCLO bit, user should execute the following sequence:

- ✧ Read contents of the SPSR register
- ✧ Perform access to the SPDR register (read or write)

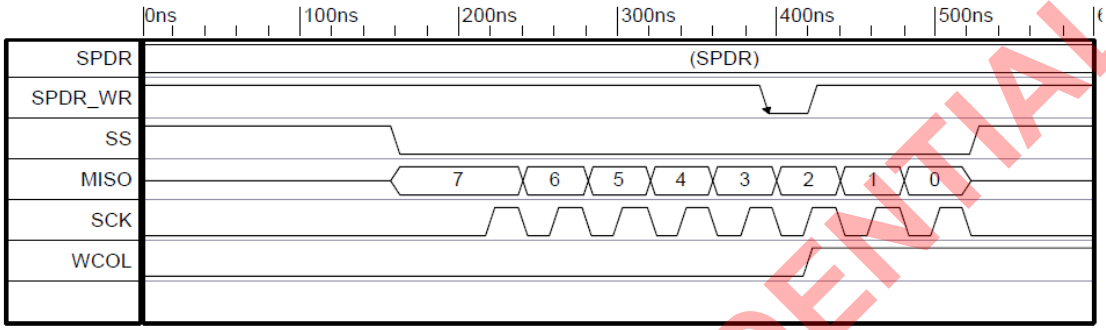


Figure16.7 Write Collision Error – SPI Slave MODE – SPDR write during transfer

Figure below shows the WCOL generation, in case that the CPHA is cleared. As it is shown the WCOL generation is cause by any S{DR register write with SS line cleared. It is done even if the SPI master didn't generate the serial clock SCK. This is because there is not clearly specified the transfer beginning, and SS driven low after full byte transfer may indicate beginning of the next byte transfer.

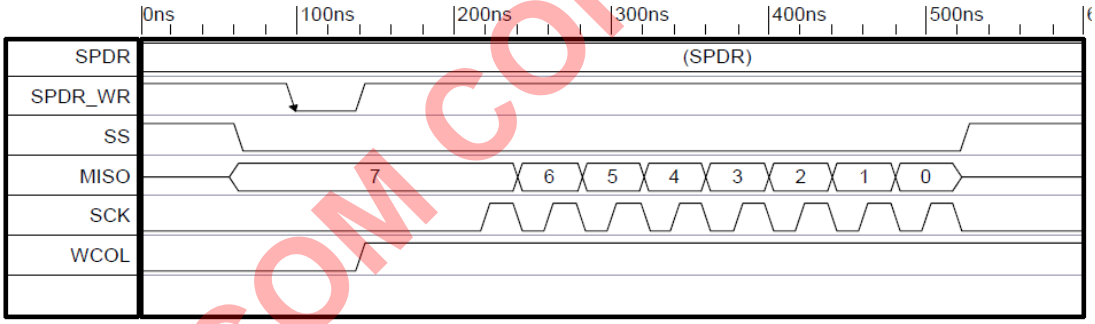


Figure16.8 WCOL Error-SPI Slave MODE-SPDR write when CPHA = 0 and SS = 0

16.6 CLOCK CONTROL LOGIC

16.6.1 SPI CLOCK PHASE AND POLARITY CONTROLS

Software can select any of four combinations of serial clock (SCK) phase and polarity using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers to allow a master device to communicate with peripheral slaves having different requirements. The flexibility of the SPI system on the SPI MODULE allows direct interface to almost any existing SYNChronous serial peripheral.

16.6.2 SPI MODULE TRANSFER FORMATS

During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line SYNChronizes shifting and sampling of the information on the two serial data lines. A slave select line allows individual selection of a slave SPI device; slave devices that are not selected do not interfere with SPI bus activities. On a master SPI device, the slave select line can optionally be used to indicate a multiple-master bus contention.

16.6.3 CPHA EQUALS ZERO TRANSFER FORMAT

Figure below shows a timing diagram of an SPI transfer where CPHA is 0. Two waveforms are shown for SCK: one for CPOL equals 0 and another for CPOL equals 1. The diagram may be interpreted as a master or slave timing diagram since the SCK, master in/slave out (MISO), and master out/slave in (MOSI) pins are directly connected between the master and the slave. The MISO signal is the output from the slave, and the MOSI signal is the output from the master. The SS line is the slave select input to the slave; the SS pin of the master is not shown but is assumed to be inactive. The SS pin of the master must be

high. This timing diagram functionally depicts how a transfer takes place; it should not be used as a replacement for data-sheet parametric information.

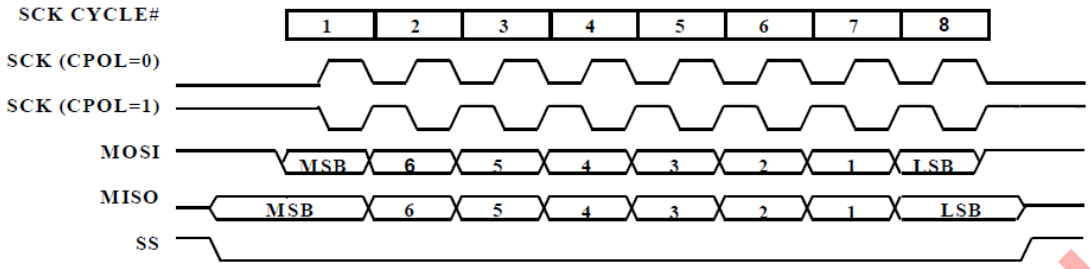


Figure16.9 CPHA Equals Zero SPI Transfer Format

When CPHA = 0, the SS line must be disserted and reasserted between each successive serial byte. Also, if the slave writes data to the SPI data register (SPDR) while SS is active low, a write-collision error results. When CPHA = 1, the SS line may remain active low between successive transfers (can be tied low at all times). This format is sometimes preferred in systems having a single fixed master and a single slave driving the MISO data line.

16.6.4 CPHA EQUALS ONE TRANSFER FORMAT

Figure below is a timing diagram of an SPI transfer where CPHA = 1. Two waveforms are shown for SCK: one for CPOL = 0 and another for CPOL = 1. The diagram may be interpreted as a master or slave timing diagram since the SCK, MISO, and MOSI pins are directly connected between the master and the slave. The MISO signal is the output from the slave, and the MOSI signal is the output from the master. The SS line is the slave select input to the slave; the SS pin of the master is not shown but is assumed to be inactive. The SS pin of the master must be high or must be reconfigured as a general-purpose output not affecting the SPI.

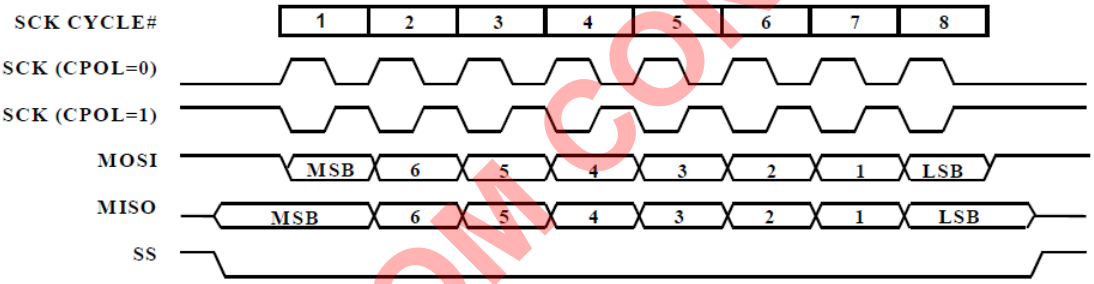


Figure16.10 CPHA Equals One SPI Transfer Format

16.7 SPI DATA TRANSFER

16.7.1 TRANSFER BEGINNING PERIOD (INITIATION DELAY)

All SPI transfers are started and controlled by a master SPI device. As a slave, the SPI MODULE considers a transfer to begin with the first SCK edge or the falling edge of SS, depending on the CPHA format selected. When CPHA = 0, the falling edge of SS indicates the beginning of a transfer. When CPHA = 1, the first edge on the SCK indicates the start of the transfer. In either CPHA format, a transfer can be aborted by taking the SS line high, which causes the SPI slave logic and bit counters to be reset. The SCK rate selected has no effect on slave operations since the clock from the master is controlling transfers.

When the SPI is configured as a master, transfers are started by a software write to the SPDR.

16.7.2 TRANSFER ENDING PERIOD

An SPI transfer is technically complete when the SPIF flag is set, but, depending on the configuration of the SPI system, there may be additional tasks. Because the SPI bit rate does not affect timing of the ending period, only the fastest rate is considered in discussions of the ending period. When the SPI is configured as a master, SPIF is set at the end of the eighth SCK cycle. When CPHA equals 1, SCK is inactive for the last half of the eighth SCK cycle.

When the SPI is operating as a slave, the ending period is different because the SCK line can be aSYNChronous to the MCU cloCKS of the slave and because the slave does not have access to as much information about SCK cycles as the master. For example, when CPHA = 1, where the last SCK edge occurs in the middle of the eighth SCK cycle, the slave has no way of knowing when the end of the last SCK cycle is. For these reasons, the slave considers the transfer complete after the last bit of serial data has been sampled, which corresponds to the middle of the eighth SCK cycle.

The SPIF flag is set at the end of a transfer, but the slave is not permitted to write new data to the SPDR while the SS line is still low.

16.8 TIMING DIAGRAMS

16.8.1 MASTER TRANSMISSION

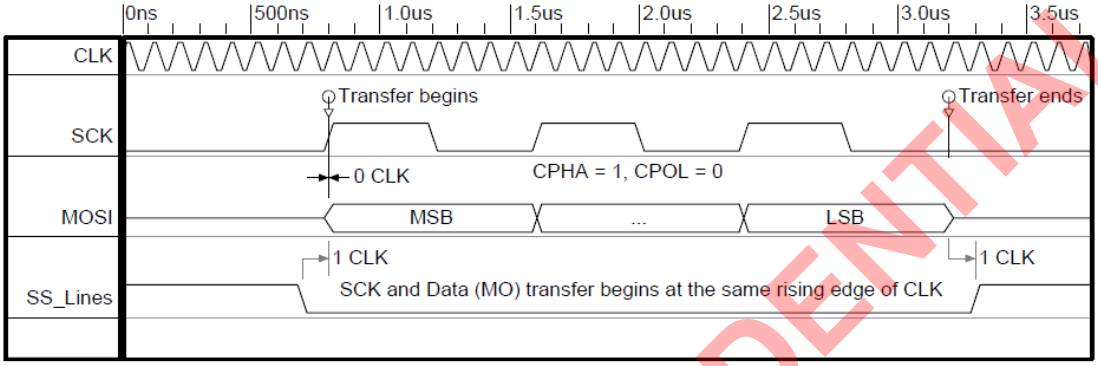


Figure16.11 Master MODE timing diagram

16.8.2 SLAVE TRANSMISSION

At a beginning of transfer in Slave MODE, the data on serial output (MISO) appears on first rising edge after falling edge on Slave Select (SS) line. Next bits of serial data are driving into MISO line on first rising edge of CLK after SKC active edge (in this case rising edge of SCK).

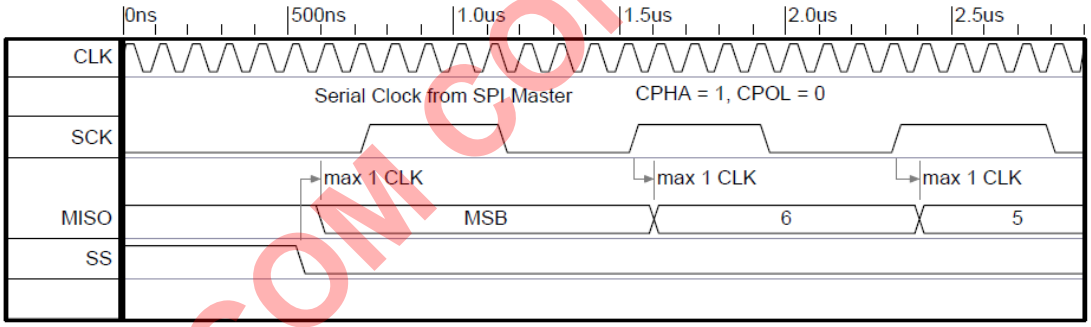


Figure16.12 Slave MODE timing diagram

16.9 SPI MODULE INTERRUPT GENERATION

When interrupt is enabled (SPIE bit in SPCR=1), SPI interrupt flag is automatically asserted when SPI transfer is completed or transfer error has occurred. SPIIF flag has to be cleared by software.

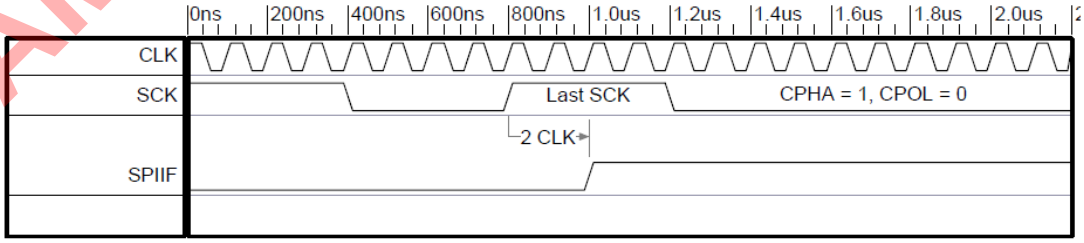


Figure16.13 Interrupt generation

Interrupt flag	Function
SPIIF	Internal, SPI

Table16.1 SPI interrupt summary

■ **SPI Interrupt state Register (Address: 0x50002008h)**

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W			Rxfifo_int_clr	Txfifo_int_clr				
R			Rxfifo_int_state	Txfifo_int_state			Rxfifo_intie	Txfifo_intie
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

RXFIFO_INTIE：SPI RXFIFO interrupt enable
TXFIFO_INTIE：SPI TXFIFO interrupt enable

T(R)X_FIFO Interrrupt State SPI T(R)X interrupt flag
T(R)X_FIFO Interrrupt Clear UART interrupt clear when write 1 to correspond to the INTSTATE
Please refer the Chapter 10.3.2 for more detail information.

17. PWM

A8137M0 has 8 channels Pulse width modulator (PWM) output. Every channel PWM has an 8-bit counter with comparator, a control register (PWMxCON) and two setting registers (PWMxH and PWMxL). User can select clock source by setting PWMxCON. Enable PWM output and function by setting PWMxEN = 1; otherwise disable PWM output and function by setting PWMxEN =0. When user set PWMxEN=0, it output LOW single and reload the PWMxL to itself. When the counter is enabled and matches the content of PWMxH, its output is asserted HIGH; when the counter is overflow, its output is asserted LOW and reload PWMxL to itself. The pulse frequency and the duty cycle for 8-bit PWM is given by the below equation

$$\text{Pulse frequency} = \text{System clock} / 2^{\text{PWMxCLK}+1} / (256\text{-PWMxL})$$
$$\text{Duty cycle} = (256\text{-PWMxH}) / 256\text{-PWMxL})$$

Noted: PWMxH must be larger then PWMxL. Otherwise, PWM output always is LOW.

17.1 PWM FUNCTIONALITY

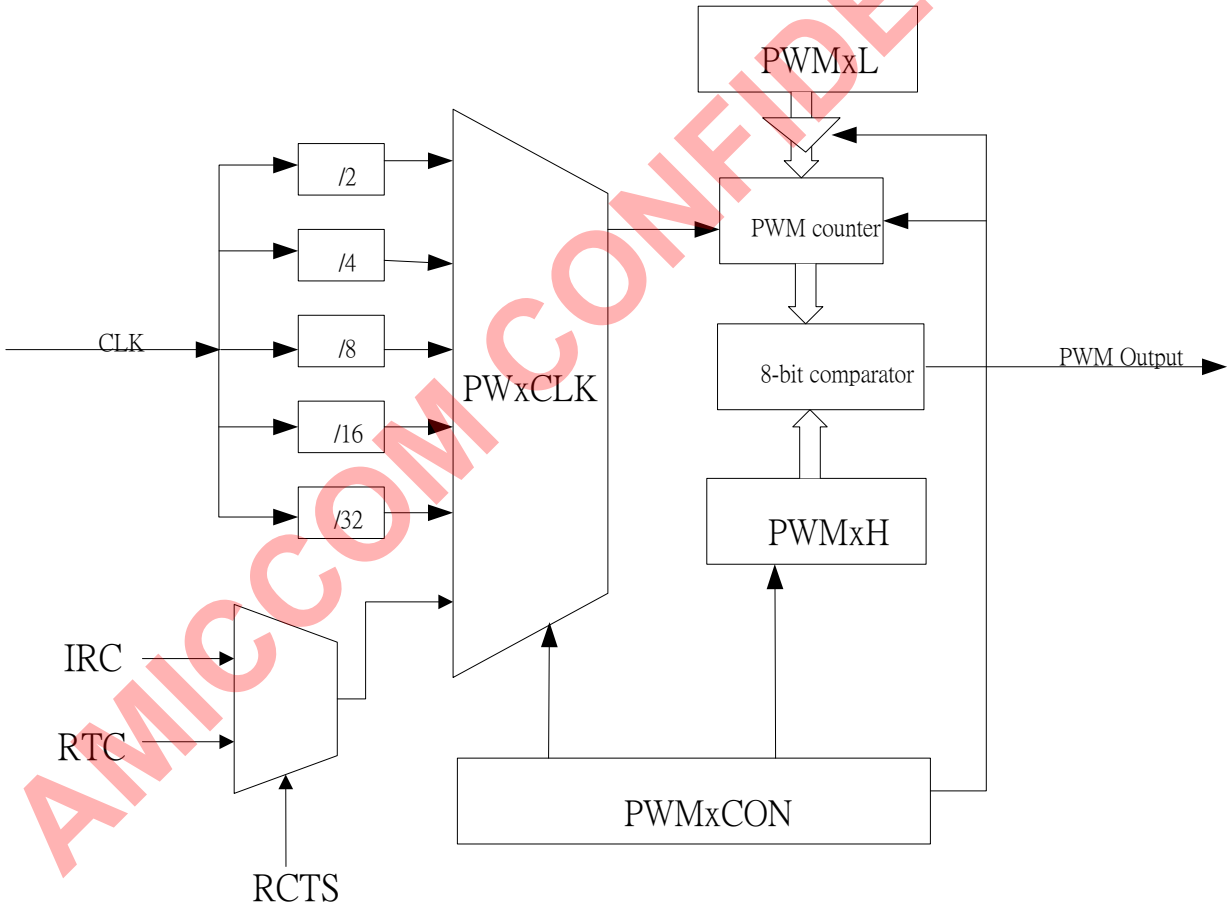


Figure17.1 PWM Block Diagram

The PWM pins functionality is described in the following table. All pins are one directional.

PIN	ACTIVE	TYPE	DESCRIPTION
PWM0(P0.20)		OUTPUT	PWM 0 output
PWM1(P0.21)		OUTPUT	PWM 1 output
PWM2(P0.10)		OUTPUT	PWM 2 output
PWM3(P0.11)		OUTPUT	PWM 3 output
PWM4(P0.12)		OUTPUT	PWM 4 output

PWM5(P0.13)		OUTPUT	PWM 5 output
PWM6(P0.14)		OUTPUT	PWM 6 output
PWM7(P0.15)		OUTPUT	PWM 7 output

Table17.1 PWM PIN define

17.1.1 PWM Control Register (Address: 0x50004000h, 0x50004100h, 0x50004200h, …. , 0x50004700h for PMW0 ~ 7)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PWMxEN	-	-	-	PWMxRTC	PWMxCLK	PWMxCLK	PWMxCLK
R	PWMxEN	-	-	-	PWMxRTC	PWMxCLK	PWMxCLK	PWMxCLK
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

PWMxEN PWMx Enable,
[0]: Disable. **[1]:** Enable.

PWMxRTC PWMx Clock Source select,
[0]: MCU Clock. **[1]:** RTC clock.

PWMxCLK PWMx Clock select
[000]: PWM Clock /2
[001]: PWM Clock / 4
[010]: PWM Clock / 8
[011]: PWM Clock / 16
[100]: PWM Clock / 32
[101]: PWM Clock / 64

17.1.2 PWM Duty Setting Register (Address: 0x50004004h, 0x50004104h, 0x50004204h, …. , 0x50004704h for PMW0 ~ 7)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PWMxL	PWMxL	PWMxL	PWMxL	PWMxL	PWMxL	PWMxL	PWMxL
R	PWMxL	PWMxL	PWMxL	PWMxL	PWMxL	PWMxL	PWMxL	PWMxL
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	PWMxH	PWMxH	PWMxH	PWMxH	PWMxH	PWMxH	PWMxH	PWMxH
R	PWMxH	PWMxH	PWMxH	PWMxH	PWMxH	PWMxH	PWMxH	PWMxH
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

PWMxH PWMx duty setting
PWMxL PWMx frequency setting

18. Watchdog Timer

A8137M0 has a special timer, called Watchdog Timer. It is a useful programmable clock counter that serves as a time-base generator, an event timer or system supervisor. User can use be a very long timer with disabled reset function.

18.1.1 Watchdog timer overview

The Watchdog Free-Running Counter (WdogFrc) is a sub-component of the Watchdog module. It essentially contains:

* The 32-bit free-running down-counter.
* Period load register.
* Control register to enable reset and interrupt signals.
* Interrupt status register.
* Lock register to prevent accidental write access.
* Interrupt and Reset generation logic.

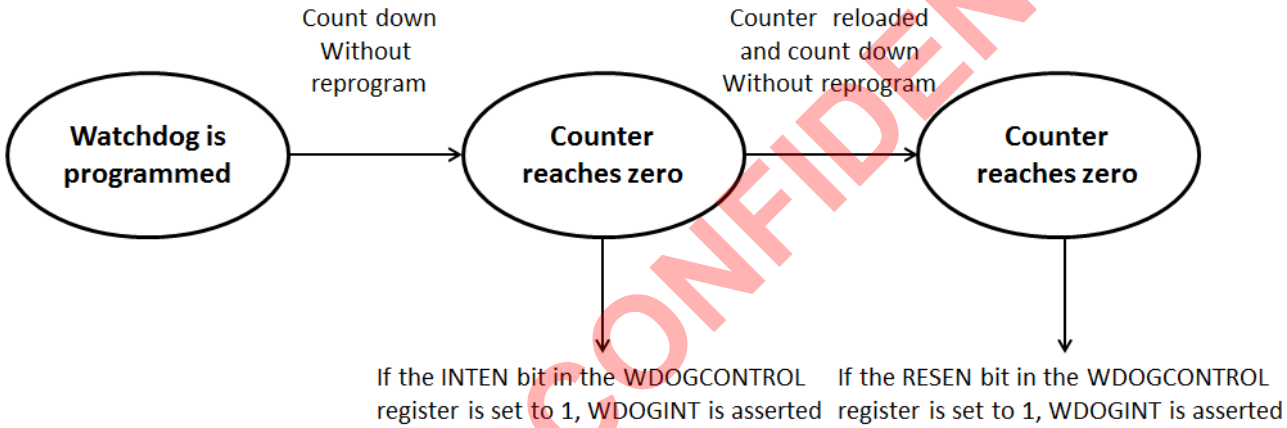


Figure 18.1 Watchdog Timer architecture.

18.1.2 Watchdog Load Register (Address: 0x40008000h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	Load	Load	Load	Load	Load	Load	Load	Load
R	Load	Load	Load	Load	Load	Load	Load	Load
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	Load	Load	Load	Load	Load	Load	Load	Load
R	Load	Load	Load	Load	Load	Load	Load	Load
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	Load	Load	Load	Load	Load	Load	Load	Load
R	Load	Load	Load	Load	Load	Load	Load	Load
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	Load	Load	Load	Load	Load	Load	Load	Load
R	Load	Load	Load	Load	Load	Load	Load	Load

LOAD The minimum valid value for WDOGLOAD is1.

18.1.3 Watchdog Value Register (Address: 0x40008004h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	Value	Value	Value	Value	Value	Value	Value	Value
R	Value	Value	Value	Value	Value	Value	Value	Value
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**

W	Value	Value	Value	Value	Value	Value	Value	Value
R	Value	Value	Value	Value	Value	Value	Value	Value
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	Value	Value	Value	Value	Value	Value	Value	Value
R	Value	Value	Value	Value	Value	Value	Value	Value
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	Value	Value	Value	Value	Value	Value	Value	Value
R	Value	Value	Value	Value	Value	Value	Value	Value

Value Watchdog value

18.1.4 Watchdog Control Register (Address: 0x40008008h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W							RESTEN	INTEN
R							RESTEN	INTEN
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

RESEN RESEN enable watchdog reset output, WDOGRES. Acts as a mask for the reset output. Set HIGH to enable the reset, or LOW to disable the reset.

INTEN INTEN enable the interrupt event, WDOGINT. Set HIGH to enable the counter and interrupt, or LOW to disable the counter and interrupt. Reloads the counter from the value in WDOGLOAD when the interrupt is enabled, after previous being disabled.

18.1.5 Watchdog Interrupt Clear Register (Address: 0x4000800Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	INTSCLR	INTSCLR	INTSCLR	INTSCLR	INTSCLR	INTSCLR	INTSCLR	INTSCLR
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	INTSCLR	INTSCLR	INTSCLR	INTSCLR	INTSCLR	INTSCLR	INTSCLR	INTSCLR
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	INTSCLR	INTSCLR	INTSCLR	INTSCLR	INTSCLR	INTSCLR	INTSCLR	INTSCLR
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W	INTSCLR	INTSCLR	INTSCLR	INTSCLR	INTSCLR	INTSCLR	INTSCLR	INTSCLR
R								

INTCLR Write any value to INTSCLR to clear WDOGINT

18.1.6 Watchdog Raw Interrupt Status Register (Address: 0x40008010h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								

R								RAWINTSTAT
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								

RAWINTSTAT Raw Watchdog Interrupt Raw interrupt status from the counter.

18.1.7 Watchdog Mask Interrupt Status Register (Address: 0x40008014h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								
R								MASKINTSTAT
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								

MASKINTSTAT Raw Watchdog Interrupt Raw interrupt status from the counter.

19. ADC (Analog to Digital Converter)

A8137M0 has built-in 8-bits / 12-bits ADC do RSSI measurement as well as carrier detection function. And It also use a general ADC and selects input source from P0.18 (PIN39), P0.19 (PIN40), P0.8 (PIN29), P0.9 (PIN30) or P0.12(PIN33) ~ P0.15(PIN36). The ADC clock (F_{ADC}) is 4MHz. The ADC converting time is 20 x ADC clock periods.

Bit		Mode	
ADCIOS0	ARSSI	Standby	RX
0	1	None	RSSI / Carrier detect
1	x	External Input	External Input

Table 18.1 Setting of ADC function

19.1 12bit ADC Control Register (Address: 0x50080000h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	BUFS12B			MODE12	MVS122	MVS121	MVS120	ADCE12
R				MODE12	MVS122	MVS121	MVS120	ADCE12
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W	ADCIOS3	ADCIOS2	ADCIOS1	ADCIOS0			ADIVL	ADCYC
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W					CKS1	CKS0	DELS1	DELS0
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

ADCIOS[3:0]: ADC I/O select.

CKS[1:0]: ADC clock selected.
[00]: 4 MHz
[01]: 2 MHz
[10]: 1 MHz
[11]: 500 kHz

ADCIOS[3:1]
[000]: Select P0.18 as the ADC analog input
[001]: Select P0.19 as the ADC analog input
[010]: Select P0.8 as the ADC analog input
[011]: Select P0.9 as the ADC analog input
[100]: Select P0.12 as the ADC analog input
[101]: Select P0.13 as the ADC analog input
[110]: Select P0.14 as the ADC analog input
[111]: Select P0.15 as the ADC analog input

ADCIOS[0]
[1]: Enable ADC analog input
[0]: Disable ADC analog input

19.2 External Input

User can use 12 Bit ADC to measure the external input. The input voltage range is from 0V ~ 1.2V. Please take care the input voltage if set the input source from external input. User can set ADCIOS[3 :1] to select input source. Set ADCIOS0 to 1 to enable external input. Refer the following formula, user calculate the input voltage from ADC[11 :0] (0x50008004h)

ADC input voltage = 1.2 * ADC [11:0] / 2048 V.

19.3 RSSI Measurement

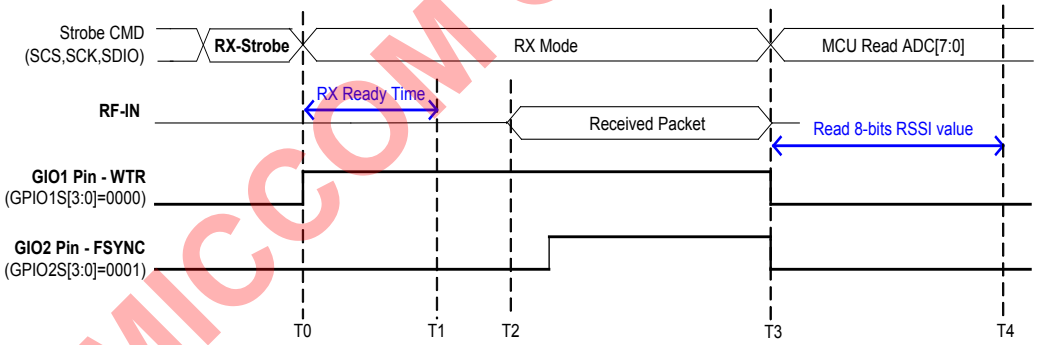
A8137M0 supports 8-bits digital RSSI to detect RF signal strength. RSSI value is stored in ADC [7:0] (0x50001244h). Fig 19.1 shows a typical plot of RSSI reading as a function of input power. This curve is base on the current gain setting of A8137M0 reference code. A8137M0 automatically averages 2/4/8/16-times (by AVGS setting) ADC conversion a RSSI measurement until A8137M0 exits RX mode. Therefore, maximum RSSI measuring time is (16 x 20 x F_{ADC}). Be aware RSSI accuracy is about ± 6dB.

Figure 19.1 Typical RSSI characteristic.

Auto RSSI measurement for TX Power:

1. Enable ARSSI= 1 (0x50001240h).
2. Send RX Strobe command.
3. In RX mode, 8-times average a RSSI measurement periodically.
4. Exit RX mode, user can read digital RSSI value from ADC [7:0] (0x50001244h) for TX power.

In step 3, if A8137M0 is set in direct mode, MCU shall let A8137M0 exit RX mode within 40 us to prevent RSSI inaccuracy.



T0-T1: Settling Time
T2-T3: Receiving Packet
T3 : Exit RX mode automatically in FIFO mode
T3-T4: MCU read RSSI value @ ADC [7:0]

Figure 18.2 RSSI Measurement of TX Power.

Auto RSSI measurement for Background Power:

1. Enable ARSSI= 1 (0x50001240h).
2. Send RX Strobe command.
3. MCU delays min. 140us.
4. Read digital RSSI value from ADC [7:0] (0x50001244h) to get background power.

5. Send other Strobe command to let A8137M0 exit RX mode.

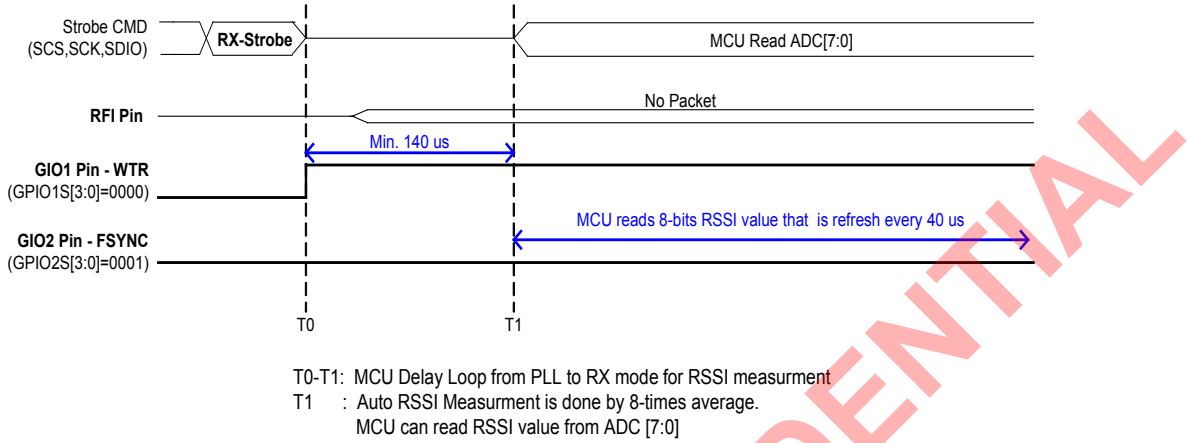


Figure 18.3 RSSI Measurement of Background Power.

19.4 Carrier Detect

Base on RSSI measurement, user can extend its application to do carrier detect (CD). In Carrier Detect mode, RSSI is refresh every 5 us without 8-times average. If RSSI level is below threshold level (RTH), CD is output high to GIO1 or GIO2 pin to inform MCU that current channel is busy.

Below is a reference procedure:

1. Set CDTH (0x50001244h)for absolute RSSI threshold level (ex. RTH = 80d).
2. Set GIO2S = [0010] (0x50001028h) for Carrier Detect to GIO2 pin.
   (2-1) Set wanted F_{RXLO} (Refer to chapter 22.5).
   (2-2) Set CDM (0x50001240, CDM =0 and hysteresis =6, or CDM =1 and hysteresis =12).
   (2-3) Enable ARSSI= 1 (0x50001240h).
   (2-4) Send RX Strobe command.
   (2-5) MCU enables a timer delay (min. 100 us).
3. MCU checks GIO2 pin.
   (3-1) If ADC $\geqq$ CDTH, GIO2 = 0.
   (3-2) If ADC $\leqq$ CDTH-CDM, GIO2 = 1.
   (3-3) If ADC locates in hysteresis zone, GIO2 = previous state.
4. Exit RX mode.

20. Battery Detect

A8137M0 has a built-in battery detector to check supply voltage (REGI pin). The detecting range is 2.0V ~ 2.7V in 8 levels.

20.1 Battery detect Register (Address: 0x50000000h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W				BLE	BDV2	BDV1	BDV0	BDE
R					BDV2	BDV1	BDV0	BDF
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

BLE: Battery life extension. Reserved for internal usage.

BDV[2:0]: Battery detection voltage.
[000]: 2.0V. **[001]:** 2.1V. [**010]:** 2.2V. **[011]:** 2.3V. **[100]:** 2.4V. **[101]:** 2.5V. [**110]:** 2.6V. **[111]:** 2.7V.

BDE: Battery detection enable.
[0]: Disable. **[1]:** Enable.

BDF: Battery detection flag.
[0]: Low Battery. **[1]:** High Battery.

When REGI < Threshold, BDF= low.
When REGI > Threshold, BDF= high.

Below is the procedure to detect low voltage input (ex. below 2.1V):

1. Set A8137 in standby or PLL mode.
2. Set BDV[2:0] (082Ch) = [001] and enable BDE (082Ch) = 1.
3. After 5 us, BDE is auto clear.
4. MCU reads BDF (082Ch).
   If REGI pin > 2.1V,
   BDF = 1 (battery high). Else, BDF = 0 (battery low).

21. Power Management

The power consumption of A8137M0 comes from two parts. One is RF part and the other is digital part (includes MCU core and peripherals). In the RF part, the sleep mode use the minimum power and the TX or RX mode use the maximum power consumptions. Use changes RF status by setting the strobe control,register(0x50001004h). For more detail information, please refer chapter 21.1. Low power operation is enabled through different power modes setting. A8137M0 has various operating mode are referred as normal mode and PM (power manager mode). Table 21.1 shows the impact of different power modes on systems operation. There are two registers to setting power manager. One is power control register (POWERCTL1, 0x50000007h).

In CKSE mode, user selects different clock be MCU core clock.in CLKSEL[2:0] then enable CKSE. User adjusts MCU clocks depends on the required power consumption. CLKSEL[2:0] = 001 ~ 110b, the MCU core clock is the clock sources divide 2 ~ 64. User could adjust the MCU speed to trade-off between the performance and the power consumption. **BEWARE, please choose CLKSEL firstly then enable CKSE to avoid glitch. Please refer the following reference code or contacts AMICCOM's FAE.**

User can enable STOP to freeze MCU core clock and all digital peripherals also stop. MCU can be waked up by hardware reset, KEY wake up, KEYINT or sleep timer (WOR /TWOR). User set sleep timer, WOR or TWOR before enter STOP mode. In this condition, it is called PM1. In PM1, all digital circuitry is stop and RF circuitry is active by WOR

Note: Please don't enable STOP and CKSE at the same time.

21.1 Power Control I Register (Address: 0x50000008h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W				PM1S-	-QD	REGAE	PM3F	STOP
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W					CLKSEL2	CLKSEL1	CLKSEL0	PMM
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W	PD_LVD					CLR	CLR	CLR
R						BODF	RESETNF	PORF
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

CLKSEL[2:0] (Clock Select), Select CKSE (Power manager mode) clock source
[000]: Clock source div 64 as MCU clock
[001]: Clock source div 2 as MCU clock
[010]: Clock source div 4 as MCU clock
[011]: Clock source div 8 as MCU clock
[100]: Clock source div 16 as MCU clock
[101]: Clock source div 32 as MCU clock
[110]: Clock source div 64 as MCU clock
[111]: Select RTC as CPU clock when CKSE=0; RTC div 2 as CPU clock when CKSE=1

PMM (Power management mode)
[1]: Enable power manager mode
[0]: Disable power manager mode

PM1S (Power Mode 1 select)
It is valid during CPU enter power mode (STOP = 1) and REGAE = 0.
[1]: Select PM1 mode.
[0]: Select PM2 mode.
The current of PM2 is similar to PM1 and PM1 is recommended for shorter settling time. Please contact AMICCOM FAE if setting about PM2.
QD (Quick discharge)
[1]: Quick discharge enable
[0]: Quick discharge disable
REGAE (Analog Regulator Enable)
It is valid during CPU enter power mode (STOP = 1).

[1]: Enable
[0]: Disable

PM3S (Power Mode 3 select)
It is valid during CPU enter power mode (STOP = 1).
[1]: Enable PM3 then VDD_D is off.
[0]: Disable PM3

STOP (Stop mode)
[1]: Enable
[0]: Disable

	MCU speed	16MHz	RAM retainance	Back to Normal	LVR	RF
Normal CKSE = 0	16MHz	ON	ON	X	X	X
Normal CKSE = 1	8/4/2/1 MHz IRC/RTC	ON	ON	X	X	X
PM1 STOP =1 REGAE = 0 PM1S = 1 PM3S = 0	OFF	OFF	ON	H/W reset / KEYINT / Sleep timer	X	OFF
PM2 STOP =1 REGAE = 0 PM1S = 0 PM3S = 0	OFF	OFF	ON	H/W reset / KEYINT / Sleep timer	X	OFF
PM3 STOP =1 REGAE=x PM1S = x PM3S = 1	OFF	OFF	OFF	H/W reset / wakeup key / Sleep timer	OFF	OFF

Table 21.1 Power manager

X: don't care, it can turn on or off by user setting

22. A8137M0 RF

A8137M0 integrate 2.4 GHz GFSK transceiver and use Strobe control register (50001004h) to control RF state. There are 6 Strobe commands to control internal state machine for RF operations. These MODEs include Sleep MODE, Idle MODE, Standby MODE, PLL MODE, RX MODE and TX MODE. There are 256Bytes FIFO for data transmitting, receiving. Sleep timer is used for WOR (Wake On Rx) and time-slotted MODE operation.

Use strobe command control RF state and user can read the RF state from MODE register

22.1 Strobe Command Register (Address: 0x50001004h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	STRB7	STRB6	STRB5	STRB4	STRB3	STRB2	STRB1	STRB0
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

STRB Strobe command register.
[0x80] Sleep MODE.
[0x90] Idle MODE.
[0xA0] Standby MODE.
[0xB0] PLL MODE.
[0xC0] TX MODE.
[0xD0] RX MODE.

Status Register (Address: 0x50001010h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								
R	CER	XER	PLLER	TRSR	TRER	RFSTATE2	RFSTATE1	RFSTATE0
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R	FPEN			CSMAF	CCAF	FPF	FECF	CRCF
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

CER: RF chip enable status.
[0]: RF chip is disabled. **[1]:** RF chip is enabled.
XER: Internal crystal oscillator enabled status.
[0]: Crystal oscillator is disabled. **[1]:** Crystal oscillator is enabled.
PLLE: PLL enabled status.
[0]: PLL is disabled. **[1]:** PLL is enabled.
TRER: TRX state enabled status.
[0]: TRX is disabled. **[1]:** TRX is enabled.
TRSR: TRX Status Register.
[0]: RX state. **[1]:** TX state.

In A8137M0, user control RF MODE as well as read/write ram. By DPTR access and MOVX instruction, user change RF MODE and know RF status.

22.1.1 Strobe Command - Sleep MODE
Refer to Strobe Control Register, user can write 0x80 to Strobe Control Register directly to set RF into Sleep MODE.

22.1.2 Strobe Command - Idle MODE
Refer to Strobe Control Register, user can write 0x90 to Strobe Control Register directly to set RF into Idle MODE.

22.1.3 Strobe Command - Standby MODE
Refer to Strobe Control Register, user can write 0xA0 to Strobe Control Register directly to set RF into Standby MODE.

22.1.4 Strobe Command - PLL MODE
Refer to Strobe Control Register, user can write 0xB0 to Strobe Control Register directly to set RF into PLL MODE.

22.1.5 Strobe Command - RX MODE
Refer to Strobe Control Register, user can write 0xC0 to Strobe Control Register directly to set RF into RX MODE.

22.1.6 Strobe Command - TX MODE
Refer to Strobe Control Register, user can write 0xD0 to Strobe Control Register directly to set RF into TX MODE.

22.2 RF Reset Command

In addition to power on reset (POR), A8137M0 could issue software reset to RF by setting RESET Register (0x50001000h). A8137M0 generates an internal signal “RESETN” to initial RF circuit. After reset command, RF state is in standby MODE and re-calibration is necessary.

22.3 FIFO Accessing Command

Before TX delivery, user only needs to write wanted data into TX FIFO (0x50001400 ~ 0x500014FF) in advance. Similarly, user can read RX FIFO (0x50001400 ~ 0x500014FF) once payload data is received. It is easy to delivery data to air. Below is the procedure of writing TX FIFO.
Step1: Send (n+1) bytes TX data in sequence by Data Byte 0, 1, 2 to n.
Step2: Send TX Strobe command for transmitting.

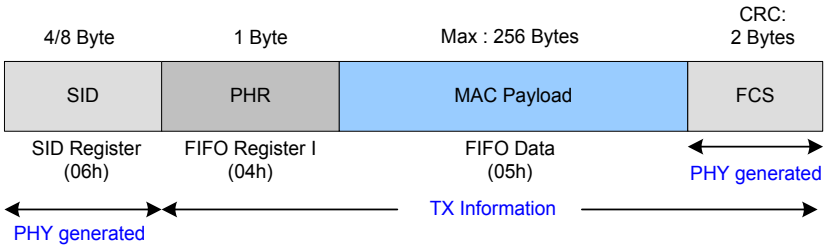
There are similar steps to read RX FIFO.
Step1: Send RX Strobe command for receiving data.
Step2: Read RX data from RX FIFO in sequence by Data Byte 0, 1, 2 to n.

A8137M0 supports separated 256-bytes TX and RX FIFO. To use A8137M0’s FIFO MODE, user just needs to enable FMS =1. For FIFO accessing, TX FIFO (write-only) and RX FIFO (read-only) share the same register address 05h. TX FIFO represents transmitted payload. On the other hand, RX circuitry SYNChronizes ID Code and stores received payload into RX FIFO.

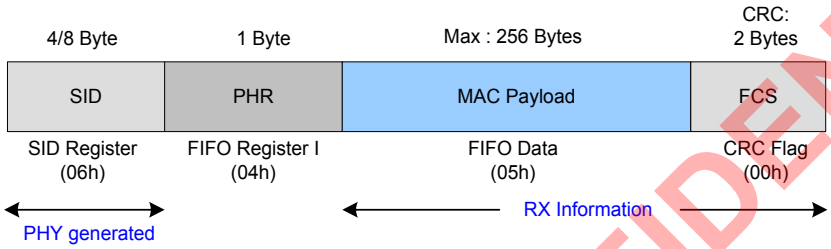
22.4 A8137M0 Frame Structure

As below TRX format, the A8137M0 contains :
- Serial Packet ID (SID:0857h~085Eh), the length is 4/8 bytes.
- The dynamic length function for PHR frame.
- The physical FIFO depth is 64 bytes and it can supports logical FIFO extension up to 256 bytes.
- If CRC is enabled (CRCS=1), 2-bytes of CRC value is transmitted automatically after payload. In the same way, RX circuitry will check CRC value and show the result to CRC Flag.

TX format



RX format



22.5 Transceiver Frequency

A8137M0 is a half-duplex transceiver with embedded PA and LNA. For TX or RX frequency setting, user just needs to set up LO frequency for two ways radio transmission.

A8137M0's main PLL features are:

- Fractional-N to generate RX/TX frequencies for all ISM 2.4 GHz channels
- Autonomous calibration loops for stable operation within the operating range
- Fast PLL settling to support frequency hopping

During receive operation, the frequency synthesizer works as a local oscillator. During transmit operation, the voltage-controlled oscillator (VCO) is directly modulated to generate the RF transmit signal. The frequency synthesizer is implemented as a fractional-N PLL.

F_{LO} = 2400 + (CHN x 0.5) in [MHz], where CHN is the channel number

A8137M0's LO frequency $F_{LO} = F_{LO\_BASE} + F_{OFFSET}$. Therefore, A8137M0 is very easy to implement frequency hopping by **ONE register setting, (CHN).** In general, user can plan the wanted channels by a CHN Look-Up-Table between master and slaves for two-way frequency hopping. Below is the LO frequency block diagram.

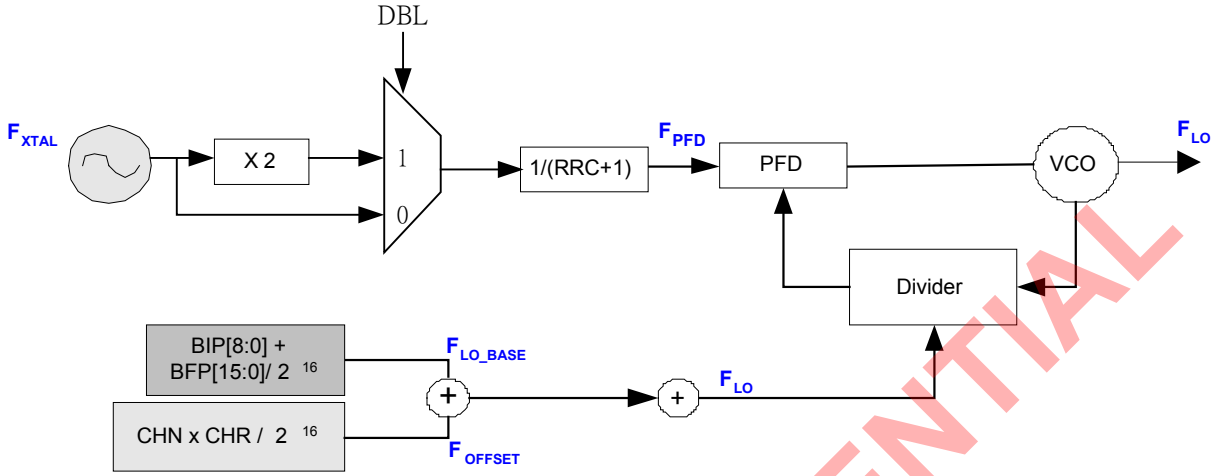


Figure 22.3 Block Diagram of Local Oscillator.

22.6 RF Clock

The master clock of A8137M0 (F_{CSCK}= 32/64 MHz) is generated by the PLL clock generator which reference frequency (F_{CGR}= 2/4 MHz) is derived from frequency divider of crystal oscillator.

$F_{CGR} = \frac{F_{XREF}}{(GRC[3:0]+1)}$, where GRC [3:0] is the divide number to get F_{CGR} from crystal oscillator.

Below is block diagram of system clock where F_{XTAL} is the crystal frequency. User can set XS, GRC, CGS to get F_{CSCK} = 32/64MHz. F_{XREF} is a reference clock to generate F_{CGR} and F_{SPLL} . After delay circuitry, F_{CSCK} (32/64MHz) is derived. And with BWS setting, the system clock F_{SYCK} can be fixed to 8MHz.

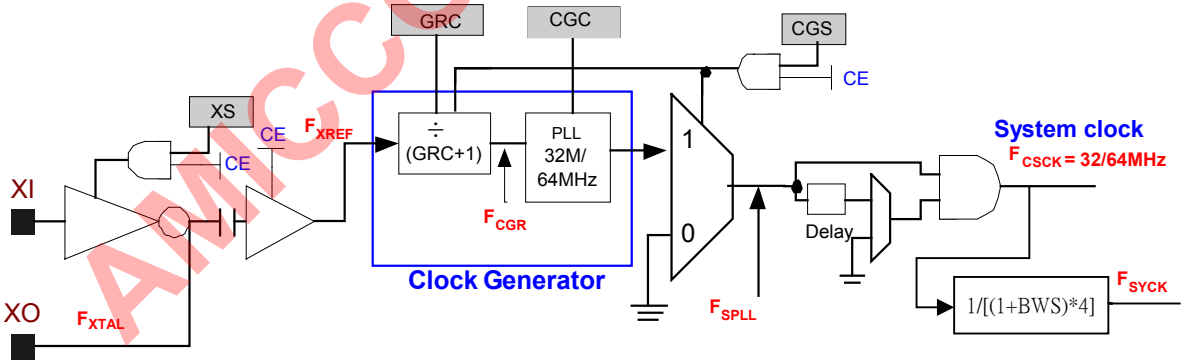


Figure 22.4 RF Clock Block Diagram.

Below is the setting table of system clock for both 1MHz and 2MHz data rate

Data rate	F_{XTAL}	F_{XREF}	F_{CGR}	GRC [3:0]	XS	CGS	CGC	BWS	F_{CSCK}	F_{SYCK}
1M	16 MHz	16 MHz	2 MHz	[0111]	1	1	0	0	32MHz	8MHz
2M	16 MHz	16 MHz	2 MHz	[0011]	1	1	1	1	64MHz	8MHz

22.7 LO Frequency Setting

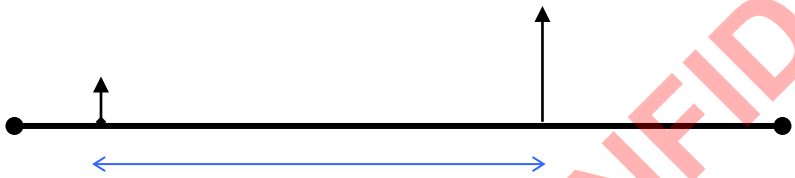
To set up 2.4GHz LO Frequency ($F_{LO,}$), user can refer to below 4 steps.

1. Set the base frequency (**F_{LO_BASE}**) by Radio Frequency Register I (0x500010C4h)
   Recommend to set **F_{LO_BASE} ~ 2400.001MHz**.

2. Set channel step F_{CHSP} = 500KHz by Radio Frequency Register I (0x500010C8h)

3. Set CHN [7:0] to get offset frequency by Channel Register I (0x500010C0h)
   F_{OFFSET} = CHN [7:0] * F_{CHSP}

4. LO frequency is equal to base frequency plus offset frequency.
   F_{LO} = F_{LO_BASE} + F_{OFFSET}



22.7.1 How to set F_{LO_BASE}

Regarding to LO frequency setting, Table 21.1 shows 2400.001 MHz base frequency by 16MHz Xtal.

STEP	ITEMS	VALUE	NOTE
1	F_{XTAL}	16 MHz	Crystal Frequency
2	BIP[7:0]	0x96	To get F_{LO_BASE} =2400 MHz
3	BFP[15:0]	0x0004	To get F_{LO_BASE} ~ 2400.001 MHz
4	F_{LO_BASE}	~2400.001 MHz	LO Base frequency

Table 22.1 How to configure F_{LO_BASE}.

22.7.2 How to set F_{LO} = F_{LO_BASE} + F_{OFFSET}

Regarding to frequency offset scheme, Table 21.2 shows Channel 11 (2405.001 MHz) by 16MHz Xtal.

STEP	ITEMS	VALUE	NOTE
1	F_{LO_BASE}	~2400.001 MHz	After cofigure BIP and BFP
2	CHR[14:0]	0x0800	To get F_{CHSP}= 500 KHz
3	CHN[7:0]	0x0A	To set channel number = 10
4	F_{OFFSET}	5 MHz	To get F_{OFFSET}= 500 KHz * (CHN) = 5MHz
5	F_{LO}	~2405.001 MHz	To get F_{LO}= F_{LO_BASE} + F_{OFFSET}

Table 22.2 How to configure F_{LO}.

22.8 State machine

In chapter 9.2 and chapter 22.1, user can learn both accessing A8137M0's control registers as well as issuing Strobe commands.

22.8.1 Key states

A8137M0 supports 6 key operation states. Those are,

(1) Standby MODE
(2) Sleep MODE
(3) Idle MODE
(4) PLL MODE
(5) TX MODE
(6) RX MODE

After power on reset or software reset or deep sleep MODE, user has to do calibration process because all control registers are in initial values. The calibration process of A8137M0 is very easy, user only needs to issue Strobe commands and enable calibration registers. After calibration, A8137M0 is ready to do TX and RX operation. User can start wireless transmission.

Strobe Command								Description
b7	b6	b5	b4	b3	b2	b1	b0	
1	0	0	0	x	x	x	x	Sleep MODE
1	0	0	1	x	x	x	x	Idle MODE
1	0	1	0	x	x	x	x	Standby MODE
1	0	1	1	x	x	x	x	PLL MODE
1	1	0	0	x	x	x	x	RX MODE
1	1	0	1	x	x	x	x	TX MODE

MODE	RF Register retention	RF Regulator	Xtal Osc.	VCO	PLL	RX	TX	Strobe Command
Sleep	Yes	ON	OFF	OFF	OFF	OFF	OFF	(1000-xxxx)b
Idle	Yes	ON	OFF	OFF	OFF	OFF	OFF	(1001-xxxx)b
Standby	Yes	ON	ON	OFF	OFF	OFF	OFF	(1010-xxxx)b
PLL	Yes	ON	ON	ON	ON	OFF	OFF	(1011-xxxx)b
TX	Yes	ON	ON	ON	ON	OFF	ON	(1101-xxxx)b
RX	Yes	ON	ON	ON	ON	ON	OFF	(1100-xxxx)b

Remark: x means “don’t care”

Table 22.3 Operation MODE and strobe command.

22.8.2 FIFO MODE

This MODE is suitable for the requirements of general purpose applications and can be chosen by setting FMS = 1. After calibration, user can issue Strobe command to enter standby MODE where write TX FIFO or read RX FIFO. From standby MODE to packet data transmission, only one Strobe command is needed. Once transmission is done, A8137M0 is auto back to standby MODE. Figure 22.4 and Figure 22.5 are TX and RX timing diagram respectively. Figure 22.6 illustrates state diagram of FIFO MODE.

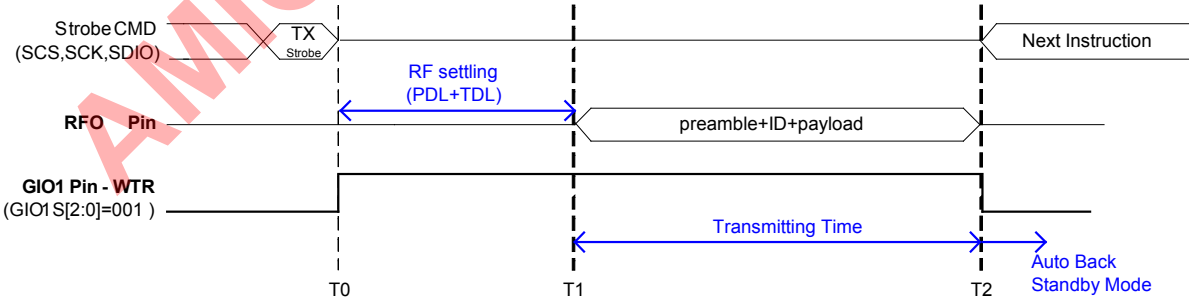


Figure 22.5 TX timing of FIFO MODE.

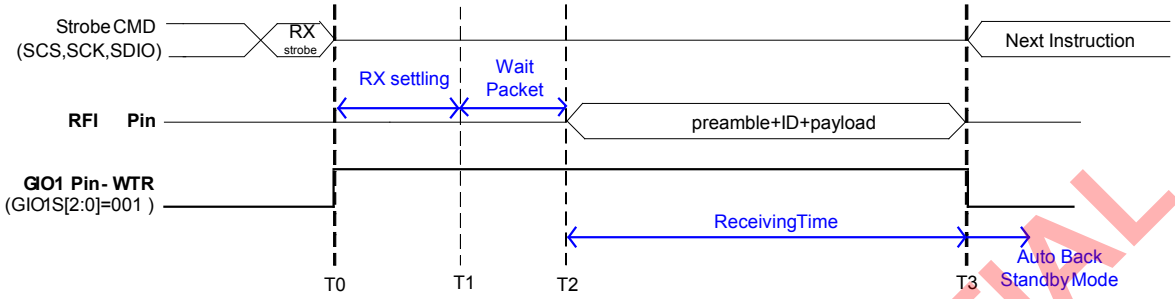


Figure 22.6 RX timing of FIFO MODE.

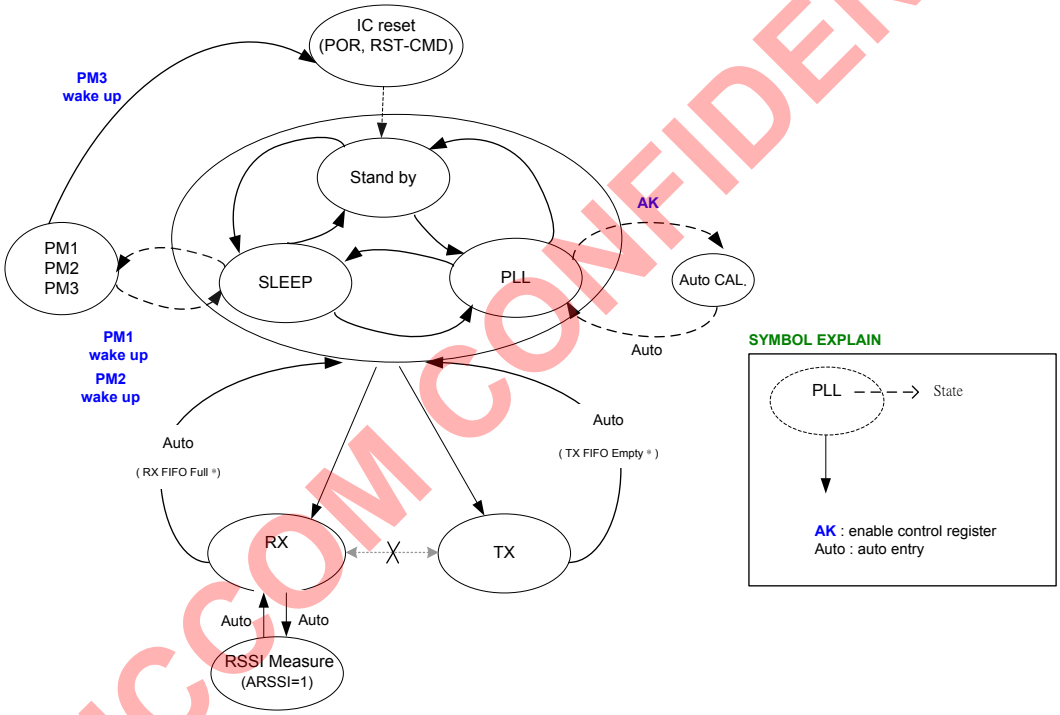


Figure 22.7 TRX State diagram

23. Flash memory controller

23.1 Flash controller command

Flash MODE register (Address: 0x4001F100)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RBB	TRIM	-	INF	TM[3]	TM[2]	TM[1]	TM[0]
R								
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

TM[3:0] (Flash Test MODE enable)

INF (Flash Information page enable)
[1]: Enable
[0]: Disable

TRIM (Flash trim MODE enable)
[1]: Enable
[0]: Disable

RBB (Flash Ready status output)
[1]: Ready
[0]: Not Ready.

Flash control register (Address: 0x4001F104)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CE			MERASE	SERASE	PERASE	PROG	WRONLY
R	CE			MERASE	SERASE	PERASE	PROG	WRONLY
R/W	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
W								
R								
R/W	**Bit 23**	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
W								
R								
R/W	**Bit 31**	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
W								
R								

WRONLY (Flash Page Write enable)
[1]: Enable
[0]: Disable

PROG (Flash Page Program internal Erase and Write enable)
[1]: Enable
[0]: Disable

PERASE (Flash Page Erase enable)
[1]: Enable
[0]: Disable

SERASE (Flash Sector Erase enable)
[1]: Enable
[0]: Disable

MERASE (Flash Mass Erase enable)
[1]: Enable
[0]: Disable

CE (Flash chip enable)
[1]: Enable
[0]: Disable

23.2 Flash controller operations

INF Truth Table

Mode	INF = Logic 1	INF= Logic 0
Read	Read the information page	Read the main memory block
Write	Write the information page	Write the main memory block
Program	Program the information page	Program the main memory block
Page Erase	Erase the information page	Erase the main memory block
Sector Erase	Erase the information page	Erase the main memory block
Mass Erase	Erase both main memory block and information page.	Erase the main memory block

Page Write
The Page Write time (T_{WR}) also includes T_{BUSY} and the internal Program cycle. During this period, the internal Program cycle will start when RBB is set at logic 0 after T_{BUSY}. This operation allows writing page function to change data from "1" to "0". The data of the selected page need to be erased by performing Page Erase, Sector Erase, or Mass Erase operation before Page Write operation. The data can be written into Assembly Buffer separately, and then be written in main memory block. The writing sequence allows up to 32 X 32 bits in a page written at the same time.
The written page cannot be re-written if Erase operation is not performed in advance; even only partial data in the selected page are written. For example, 8 X 32 bits are written into the selected page by using Page Write command. After this command has been done, the rest 24 X 32 bits cannot be written into the same selected page if Page Erase command is not performed in advance. It is suggested to use Page Write command to change whole page data.
Page/Sector/Mass Erase
Since in Page Write operation, the data will be changed to "0", Erase operations should be applied before the Page Write operation to reset all the data back to "1". The whole data in a page, a sector or all the main memory can be erased at a time by performing Page Erase, Sector Erase, or Mass Erase sequences accordingly.
Ready/Busy Port (RBB) During a Write, Program, Erase Cycle
The RBB port provides status of internal operations (Page Write, Page Program, Page Erase, Sector Erase, Mass Erase, Power On Reset, and Low Standby MODEs). Users can know whether the eFlash macro is ready to serve next command by monitoring the RBB. Any other commands are ignored while the RBB is at logic 0 state.

24. Charger

24.1 Charge cycle

The charge cycle of charger is depicted in Figure 24.1 where 1C charge current can be set by the resistor connected to VRCC pin as below.

$$I_{1c} = \frac{1.2V}{R_{VRCC}} * 1000$$

24.1.1 Trickle Charge Mode
If battery voltage < Trickle Charge Threshold Voltage, charger is in Trickle Charge mode and charge current is 0.1C.

24.1.2 Ramp Current Charge Mode
When battery voltage is between Trickle Charge Threshold Voltage and Float voltage, charger enters Ramp Current Charge Mode and charge current is from 1.1C to 1C.

24.1.3 Constant Voltage Charge Mode
When battery voltage reaches Float Voltage, charger switches to Constant Voltage Charge Mode. In this mode, battery voltage keeps constant but charge current decays gradually.

24.1.4 Standby Mode
Once charge current reduces to 0.1C during Constant Voltage Charge Mode, charge is stopped and charger enters Standby Mode.

24.1.5 Re-Charge Mode
If battery voltage drops to Re-Charge Voltage at Standby Mode interval, Re-Charge Mode is active and re-starts charge cycle.

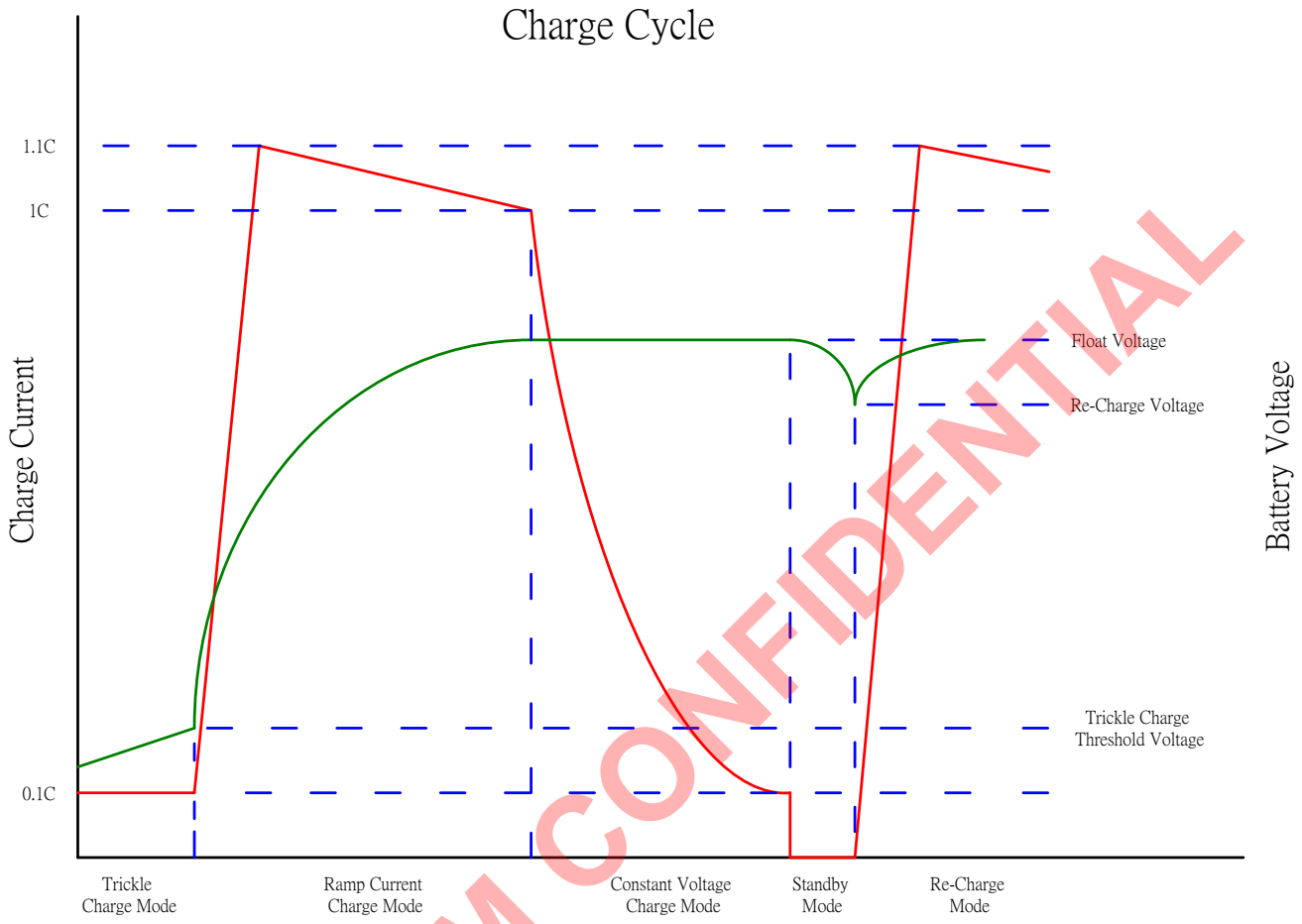


Figure 24.1 Charge cycle

24.2 Charge Protection

If beyond default threshold is detected during charge cycle, protection is triggered. In such case, charger enters Standby Mode to stop charge and associated protection flag is active.

24.2.1Over-Temperature Protection (OTP)

OTP is triggered if temperature is beyond the threshold which can be set by external thermistor. Please contact AMICCOM's FAE for more detail.

24.2.2 Over-Voltage Protection (OVP)

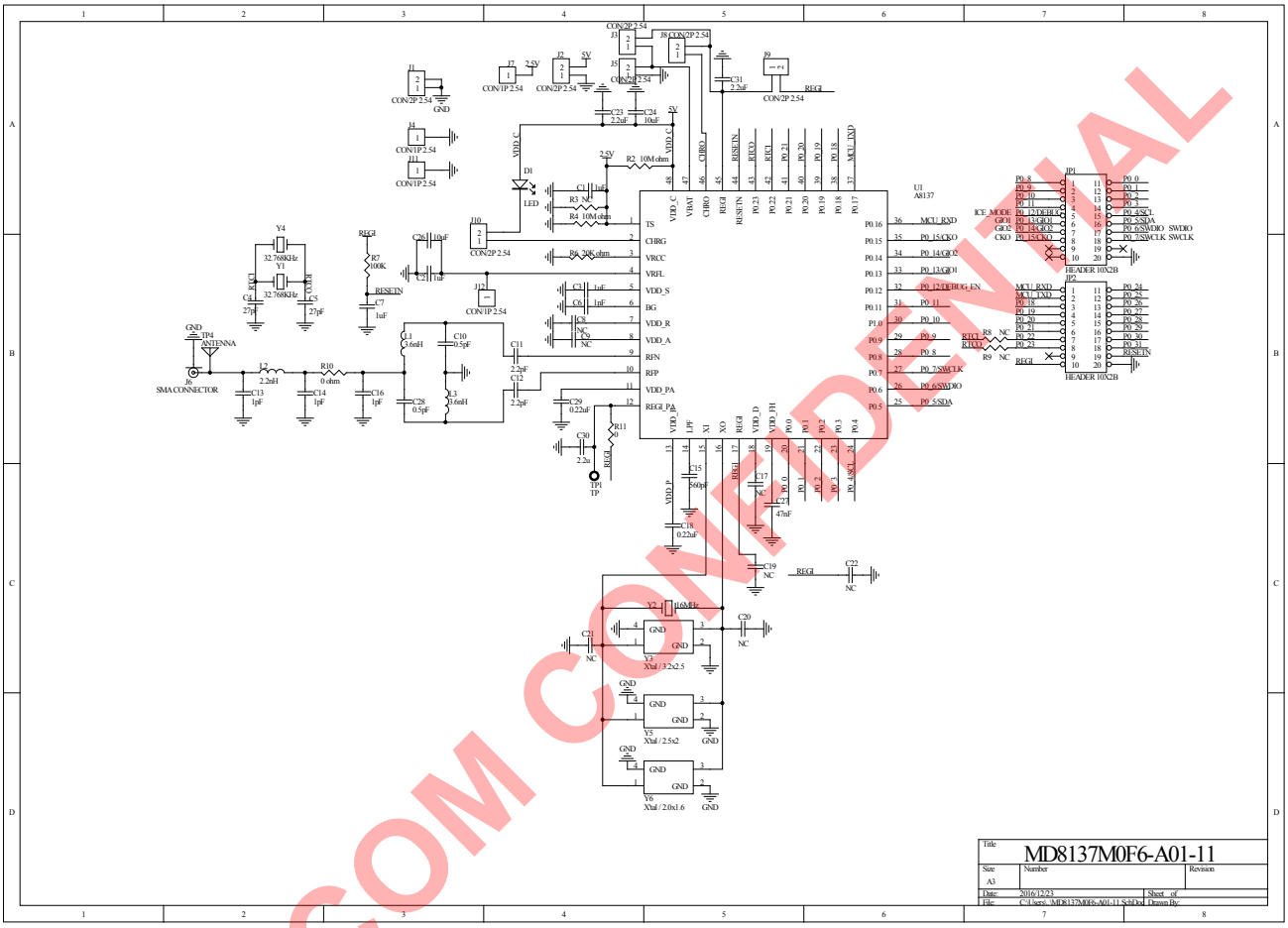
OVP is triggered if V_{BAT} > 4.5V.

24.2.3 Over-Current Protection (OCP)

OCP is triggered if I_{BAT} > 300mA.

25. Application circuit

Below are AMICCOM's ref. design circuits. For more details, please refer AMICCOM standard module , MDA8137M0-Axx.



26. Abbreviations

ADC	Analog to Digital Converter
AIF	Auto IF
FC	Frequency Compensation
AGC	Automatic Gain Control
BER	Bit Error Rate
BW	Bandwidth
CD	Carrier Detect
CHSP	Channel Step
CRC	Cyclic Redundancy Check
CODEC	Coder and Decoder
DAC	Digital to Analog Converter
DC	Direct Current
FEC	Forward Error Correction
FIFO	First in First out
FSK	Frequency Shift Keying
ID	Identifier
ICE	In Circuit Emulator
IF	Intermediate Frequency
ISM	Industrial, Scientific and Medical
LO	Local Oscillator
MCU	Micro Controller Unit
PFD	Phase Frequency Detector for PLL
PLL	Phase Lock Loop
POR	Power on Reset
PWM	Pulse width modulation
RX	Receiver
RXLO	Receiver Local Oscillator
RSSI	Received Signal Strength Indicator
SPI	Serial to Parallel Interface
SYCK	System Clock for digital circuit
TX	Transmitter
TXRF	Transmitter Radio Frequency
VCO	Voltage Controlled Oscillator
XOSC	Crystal Oscillator
XREF	Crystal Reference frequency
XTAL	Crystal

27. Ordering Information

Part No.	Package	Units Per Reel / Tray
A81U37F6101AQ6C/Q	QFN6x6, Pb Free, Tape & Reel, -40℃～85℃	3K
A81U37F6101AQ6C	QFN6x6, Pb Free, Tray, -40℃～85℃	490EA

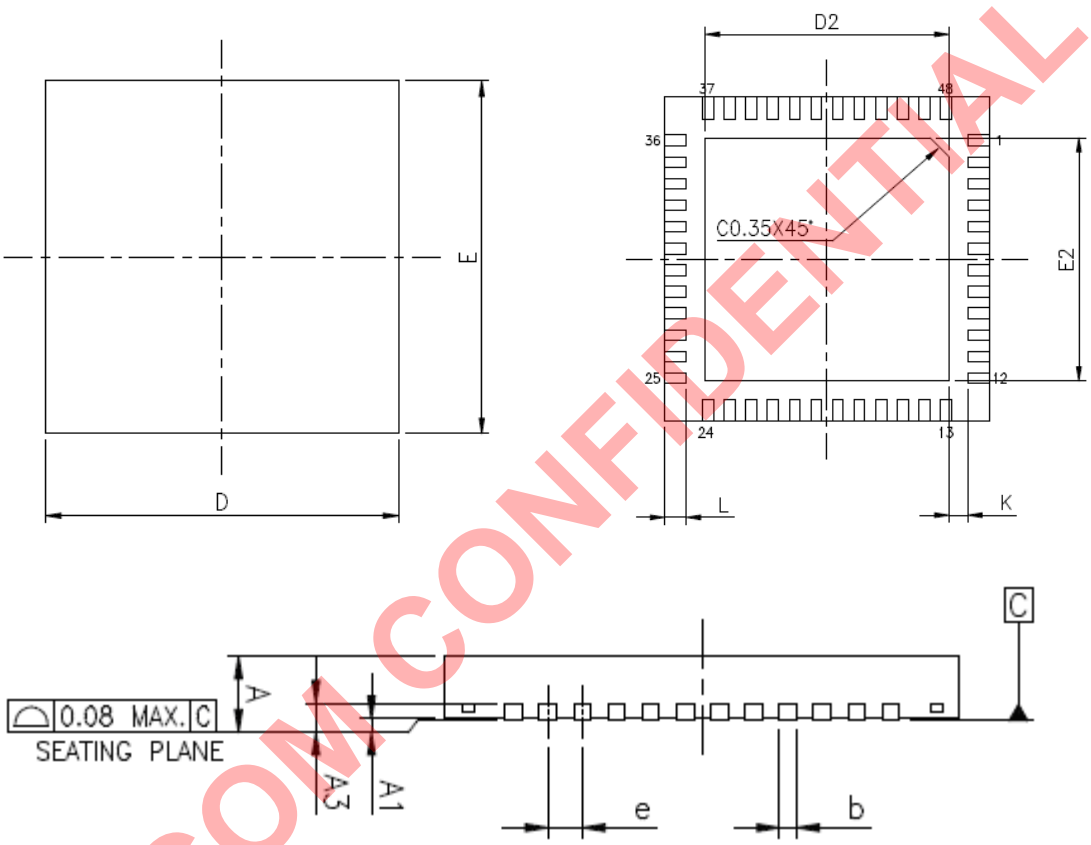
28. Package Information

QFN6*6 48L Outline Dimensions

unit: inches/mm

Top View

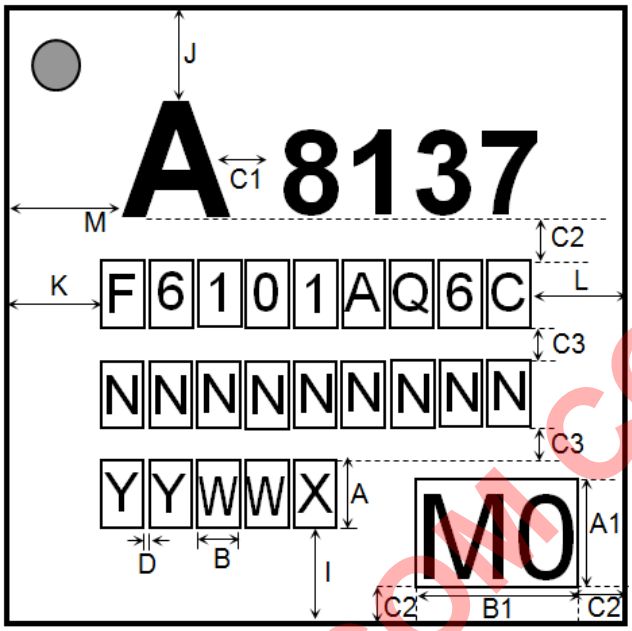
Bottom View



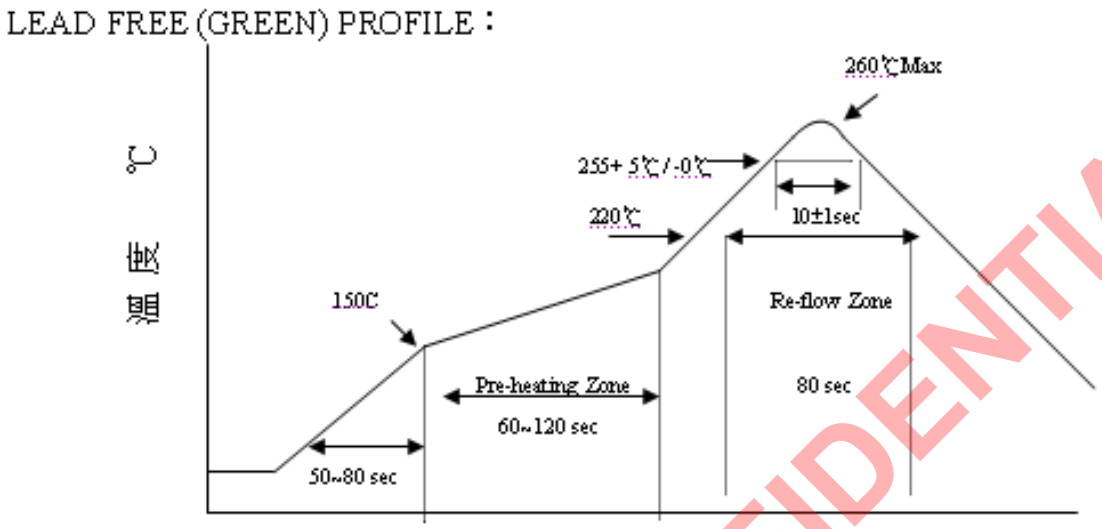
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.028	0.030	0.031	0.7	0.75	0.8
A_1	0	0.001	0.002	0.00	0.02	0.05
A_3		0.009 REF.			0.23REF.	
b	0.006	0.008	0.010	0.15	0.2	0.25
D		0.240			6.1 BSC	
D_2	0.146	0.177	0.179	3.70	4.50	4.55
E		0.240			6.1BSC	
E_2	0.146	0.177	0.179	3.70	4.50	4.55
e		0.016BSC			0.4BSC	
L	0.013	0.016	0.020	0.32	0.4	0.50
K	0.008	-	-	0.2	-	-

29. Top Marking Information

- Part No. : **A81U37F6101AQ6C**
- Pin Count : **48**
- Package Type : **QFN**
- Dimension : **6*6 mm**
- Mark Method : **Laser Mark**
- Character Type : **Arial**



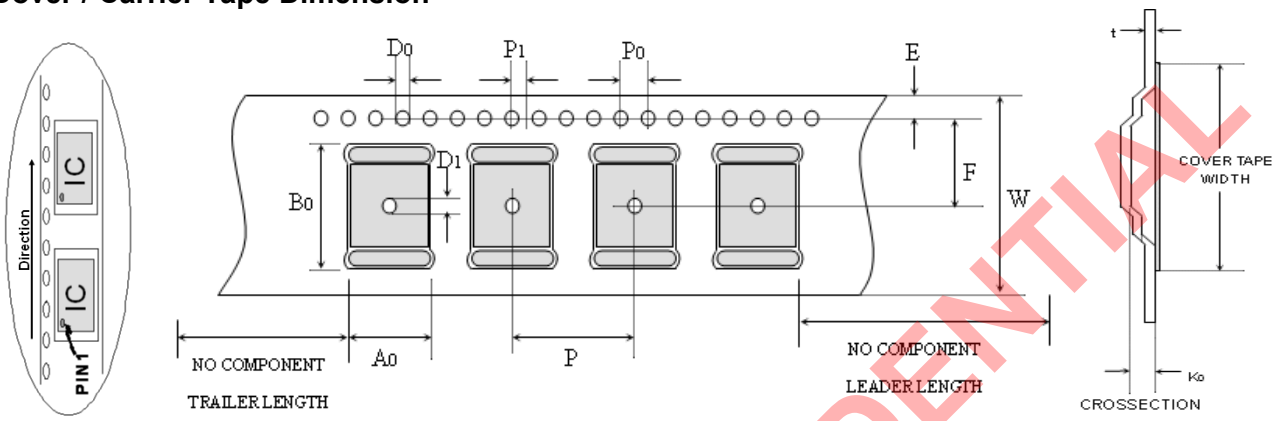
30. Reflow Profile



Actual Measurement Graph

31. Tape Reel Information

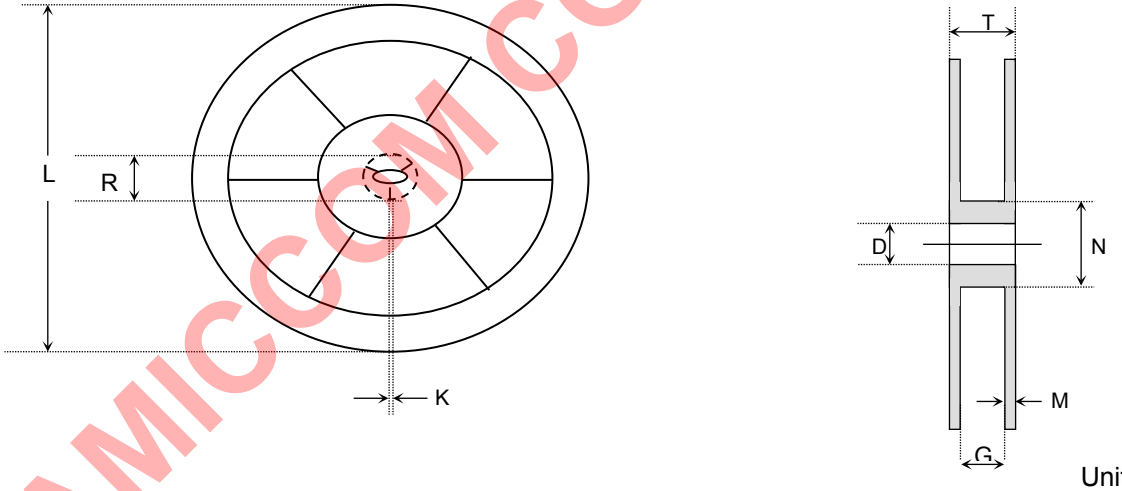
Cover / Carrier Tape Dimension



Unit: mm

TYPE	P	A0	B0	P0	P1	D0	D1	E	F	W	K0	t	Cover tape width
QFN 6*6	12±0.1	6.3±0.1	6.3±0.1	4±0.2	2±0.1	1.5±0.1	1.5±0.5	1.75 ±0.1	7.5 ±0.1	16±0.3	1.15 ±0.2	0.3 ±0.05	13.3± 0.1

REEL DIMENSIONS



Unit: mm

TYPE	G	N	M	D	K	L	R
QFN6*6	17±0.5	102 REF±2.0	2.3±0.2	13.15±0.35	2.0±0.5	330±3.0	19.6±2.9

32. Product Status

Data Sheet Identification	Product Status	Definition
Objective	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification	Noted Full Production	This data sheet contains the final specifications. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by AMICCOM. The data sheet is printed for reference information only.

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