

Document Title

A8125M0 Data Sheet, 2.4GHz FSK/GFSK low power SoC

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Issue Date</u>	<u>Remark</u>
0.0	Initial issue.	Apr., 2017	Objective
0.1	Change SRAM to 32KB. Add AES-128, VDD_I pin. Add QFN5x5 40L package and update pin configuration, pin description, chip block diagram. Modify PM mode current, TX current. Change Flash to 128KB, sleep timer x2. Modify 12 bit ADC sampling frequency spec. Add Tag function, deep sleep mode. Modify Chapter 20 ~ 23. Add IRC clock formula. Update application circuit.	Dec., 2018	Preliminary

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1. General Description

A8125M0 is a high performance and low cost 2.4GHz ISM band FSK/GFSK wireless SoC. It integrates M0 micro controller, 128KBytes flash memory and 32KBytes SRAM.

For packet handling, A8125M0 has built-in separated 64-bytes TX/RX FIFO for data buffering and burst transmission, auto-ack and auto-resend, CRC for error packet filtering, FEC for 1-bit data correction per code word, RSSI for clear channel assessment, thermal sensor for monitoring relative temperature, WOR (Wake on RX) function to support periodically wake up from sleep mode to RX mode and listen for incoming packets without MCU interaction. In addition, A8125M0 has built-in AES128 co-processor (Advanced Encryption Standard) for advanced data encryption or decryption which consists of the transformation of a 128-bit block into an encrypted 128-bit block. Those functions are very easy to use while developing a wireless system.

For low current consumption, A8125M0 is integrated with both LDO and DC-DC (buck) so that this device can be operated more efficient. User can configure one of them (LDO or DC-DC) as a powered source for device operations.

2. Typical Applications

- Wireless sensor network
- 2.4GHz active RFID
- 2.4GHz ISM system
- Smart remote controller
- Home and building automation
- Wireless toys and game controllers

3. Features

RF

- Frequency band: 2400 – 2500MHz.
- FSK and GFSK modulation
- High sensitivity:
 - ◆ -96dBm at 500Kbps data rate
 - ◆ -93dBm at 1Mbps data rate
 - ◆ -90dBm at 2Mbps data rate
- Programmable data rate 8K ~ 2Mbps
- Fast settling time synthesizer for frequency hopping system
- Support 16MHz crystal
- Easy to use.
 - ◆ Change frequency channel by one register setting
 - ◆ 8-bits Digital RSSI for clear channel indication
 - ◆ Auto RSSI measurement
 - ◆ Auto WOR (wake up when receive RX packet)
 - ◆ Auto WOT (wake up to transmit TX packet)
 - ◆ Auto Calibrations
 - ◆ Auto IF function
 - ◆ Auto Frequency Compensation
 - ◆ Auto CRC Check and filtering
 - ◆ Separated 64 bytes RX and TX FIFO
 - ◆ Support logical FIFO extension up to 256 bytes
 - ◆ Auto-ACK and Auto-resend scheme
 - ◆ Clear channel assessment (CCA)
 - ◆ Support ED (Energy Detect) for CCA
 - ◆ Auto CSMA-CA

Low Power

- Wide Range Operation Voltage from 2.0V ~ 3.6V
- RX current consumption with MCU stop and DC-DC turn on: 7.1mA @VDD_IO= 3.3V
- TX current consumption with MCU stop and DC-DC turn on: 9.2mA @ 5dBm, VDD_IO=3.3V
- Power saving MODE without sleep timer, 1KB SRAM retention (1.7uA)
- Power saving MODE with sleep timer, 1KB SRAM retention (2uA)

Microcontroller

- High performance ARM-M0 MCU
- 128KB Flash memory with copy protection, 32KB SARM

Peripherals

- Three UART, one I²C, two SPI serial communication
- Operation clock: 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 of crystal oscillator
- Two 32-bit timers and one 32-bit dual mode timer
- 8 channels PWM
- Watchdog timer
- Two 24-bit Sleep timer by IRC
- In-Circuit Debugger
- In-System programming/ In-Application programming
- 24 GPIO and Key wake-up
- Built-in thermal sensor for monitoring relative temperature
- Built-in eight channels 12-bits ADC for general purpose analog input
- Built-in Low Battery Detector
- Built-in AES128 co-processor

Tag

- Support ISO14443 type-A PICC
- Data rate: 106Kbps
- Integrate load modulation capacitor
- 7 Byte UID

Layout

- Package size: QFN5x5 40 pins / QFN6x6 48 pins

4. Pin Configurations

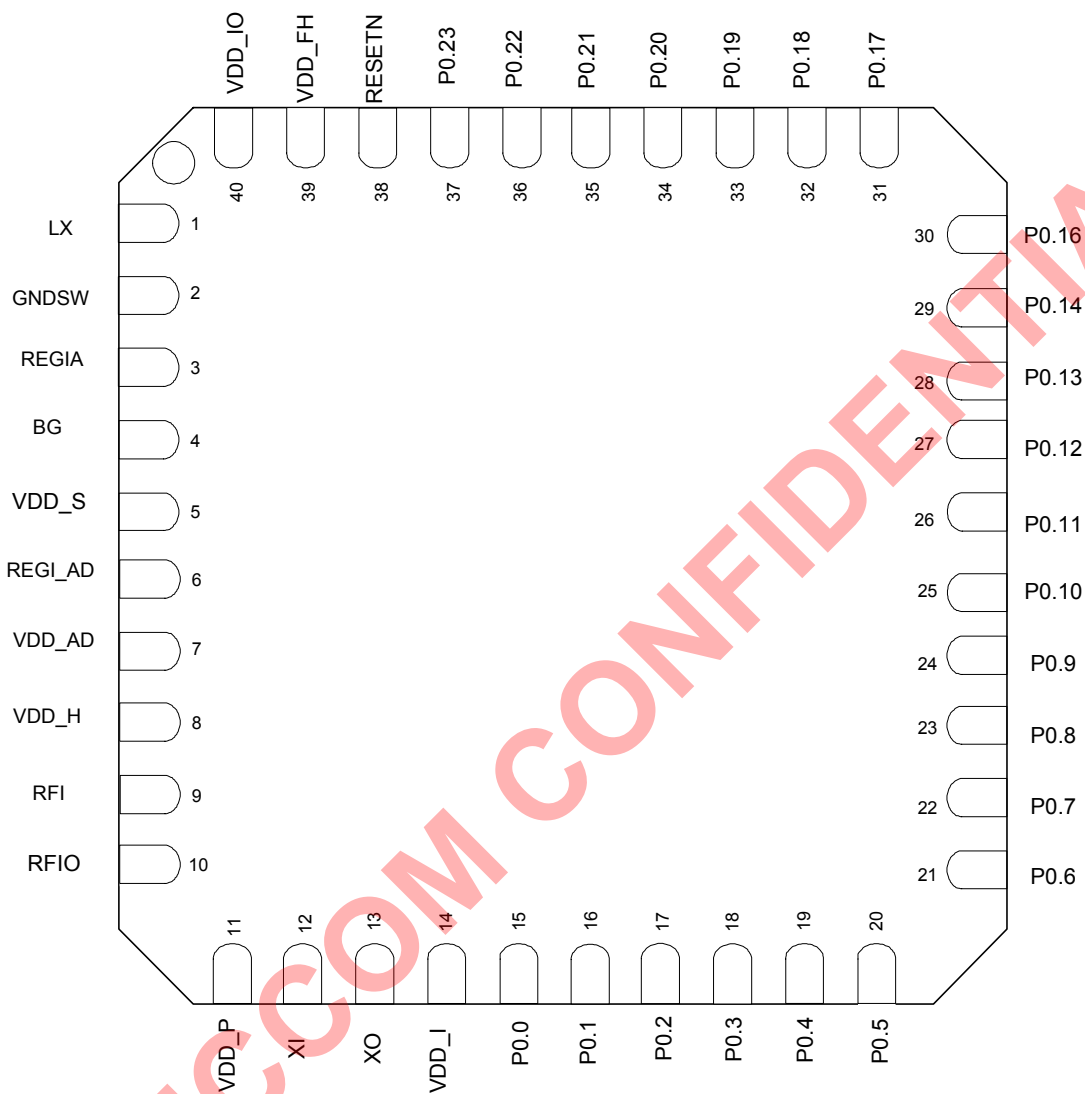


Figure 4.1 A8125M0 QFN 5x5 40 pin Package Top View

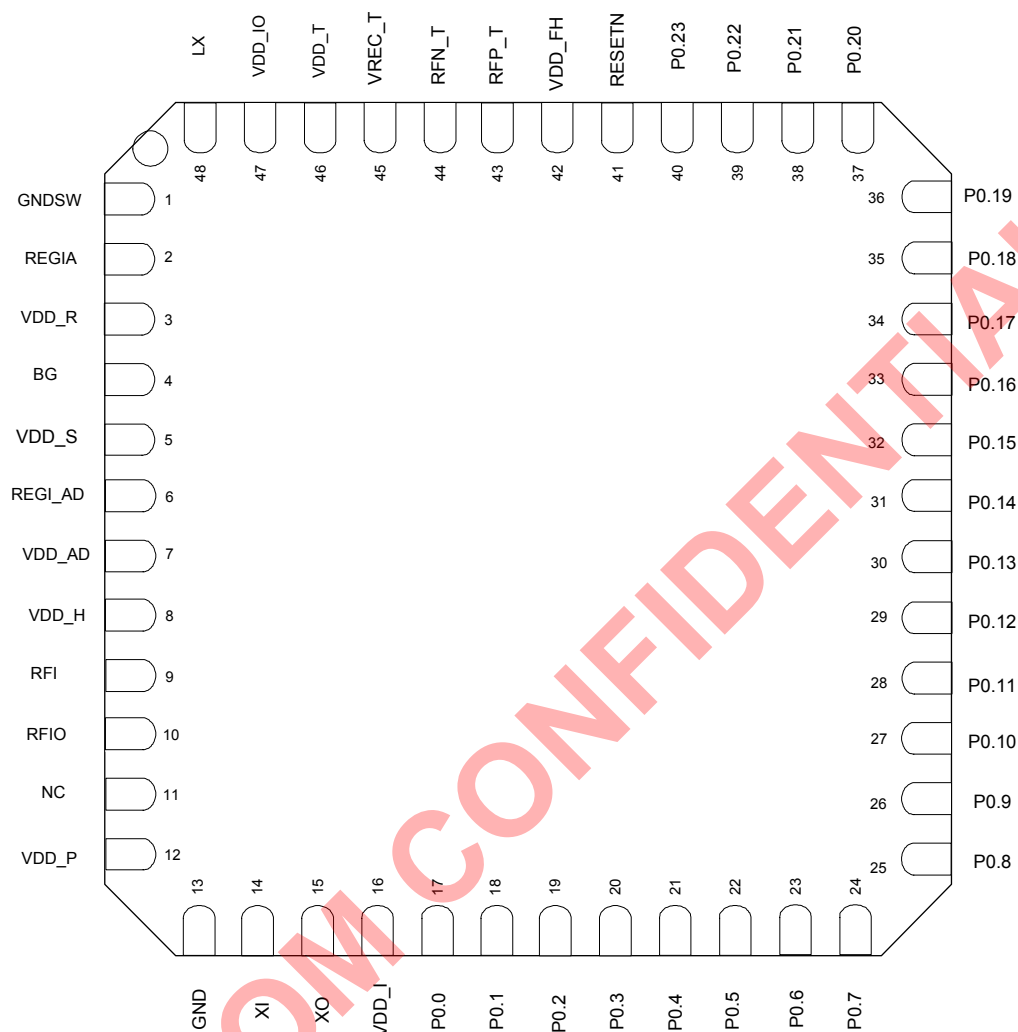


Figure 4.2 A8125M0 QFN 6x6 48 pin Package Top View

5. Pin Descriptions (I: input; O: output, I/O: input or output)

Pin No.	Symbol	I/O	Function Description
1	LX	AIO	DC-DC Inductor connection pin.
2	GNDSW	G	Ground.
3	REGIA	AO	DC-DC regulator output for buck.
4	BG	AO	Band gap output.
5	VDD_S	AO	VDD_S supply voltage output.
6	REGI_AD	AI	AD regulator input.
7	VDD_AD	AO	VDD_AD supply voltage output.
8	VDD_H	AI	VDD_H supply voltage input.
9	RFI	AI	RF input.
10	RFIO	AIO	RF input/output.
11	VDD_P	AO	PLL supply voltage output.
12	XI	AIO	Crystal oscillator input.
13	XO	AO	Crystal oscillator output.
14	VDD_I	AO	VDD_I supply voltage output.
15	P0.0	DIO	SPI0_CS
16	P0.1	DIO	SPI0_MISO
17	P0.2	DIO	SPI0_MOSI
18	P0.3	DIO	SPI0_SCK
19	P0.4	DIO	I ² CL
20	P0.5	DIO	I ² CD
21	P0.6	DIO	SWDIOTMS
22	P0.7	DIO	SWCLKTCK
23	P0.8	DIO/AI	Timer0_EIN/ADC2/ SPI1_MOSI
24	P0.9	DIO/AI	Timer1_EIN/ADC3/ SPI1_MISO
25	P0.10	DIO	PWM2/ SPI1_CS
26	P0.11	DIO	PWM3/ SPI1_SCK/BB_CKO
27	P0.12	DIO/AI	PWM4/ADC4/ICE_MODE
28	P0.13	DIO/AI	PWM5/ADC5/BB_GIO1
29	P0.14	DIO/AI	PWM6/ADC6/BB_GIO2
30	P0.16	DIO	UART0_RX
31	P0.17	DIO	UART0_TX
32	P0.18	DIO/AI	UART1_RX/ADC0/RCADC_RS
33	P0.19	DIO/AI	UART1_TX/ADC1/RCADC_RT
34	P0.20	DIO	UART2_RX/PWM0/RCADC_CS
35	P0.21	DIO	UART2_TX/PWM1/RCADC_IN
36	P0.22	DIO/AI	RTCI
37	P0.23	DIO/AO	RTCO
38	RESETN	DI	RESETN input.
39	VDD_FH	AO	Flash high voltage output.
40	VDD_IO	AI	VDD_IO supply voltage input.
	Back side plate	G	Ground. Back side plate shall be well-solder to ground; otherwise, it will impact RF performance.

Table 5.1 A8125M0 QFN5x5 40 pins

Pin No.	Symbol	I/O	Function Description
1	GNDSW	G	Ground.
2	REGIA	AO	DC-DC regulator output for buck.
3	VDD_R	AO	Auxiliary supply for 8 bit ADC input circuit.
4	BG	AO	Band gap output.
5	VDD_S	AO	VDD_S supply voltage output.
6	REGI_AD	AI	AD regulator input.
7	VDD_AD	AO	VDD_AD supply voltage output.
8	VDD_H	AI	VDD_H supply voltage input.
9	RFI	AI	RF input.
10	RFIO	AIO	RF input/output.
11	NC		
12	VDD_P	AO	PLL supply voltage output.
13	GND	G	Ground.
14	XI	AIO	Crystal oscillator input.
15	XO	AO	Crystal oscillator output.
16	VDD_I	AO	VDD_I supply voltage output.
17	P0.0	DIO	SPI0_CS
18	P0.1	DIO	SPI0_MISO
19	P0.2	DIO	SPI0_MOSI
20	P0.3	DIO	SPI0_SCK
21	P0.4	DIO	I ² CL
22	P0.5	DIO	I ² CD
23	P0.6	DIO	SWDIOTMS
24	P0.7	DIO	SWCLKTCK
25	P0.8	DIO/AI	Timer0_EIN/ADC2/ SPI1_MOSI
26	P0.9	DIO/AI	Timer1_EIN/ADC3/ SPI1_MISO
27	P0.10	DIO	PWM2/ SPI1_CS
28	P0.11	DIO	PWM3/ SPI1_SCK/BB_CKO
29	P0.12	DIO/AI	PWM4/ADC4/ICE_MODE
30	P0.13	DIO/AI	PWM5/ADC5//BB_GIO1
31	P0.14	DIO/AI	PWM6/ADC6/BB_GIO2
32	P0.15	DIO/AI	PWM7/ADC7BB_CKO
33	P0.16	DIO	UART0_RX
34	P0.17	DIO	UART0_TX
35	P0.18	DIO/AI	UART1_RX/ADC0/RCADC_RS
36	P0.19	DIO/AI	UART1_TX/ADC1/RCADC_RT
37	P0.20	DIO	UART2_RX/PWM0/RCADC_CS
38	P0.21	DIO	UART2_TX/PWM1/RCADC_IN
39	P0.22	DIO/AI	RTCI
40	P0.23	DIO/AO	RTCO
41	RESETN	DI	RESETN input.
42	VDD_FH	AO	Flash high voltage output.
43	RFP_T	AIO	Tag positive RF IO.
44	RFN_T	AIO	Tag negative RF IO.
45	VREC_T	AO	Tag rectifier output.
46	VDD_T	AO	VDD_T supply voltage output.
47	VDD_IO	AI	VDD_IO supply voltage input.
48	LX	AIO	DC-DC Inductor connection pin.
	Back side plate	G	Ground. Back side plate shall be well-solder to ground; otherwise, it will impact RF performance.

Table 5.2 A8125M0 QFN6x6 48 pins

6. Chip Block Diagram

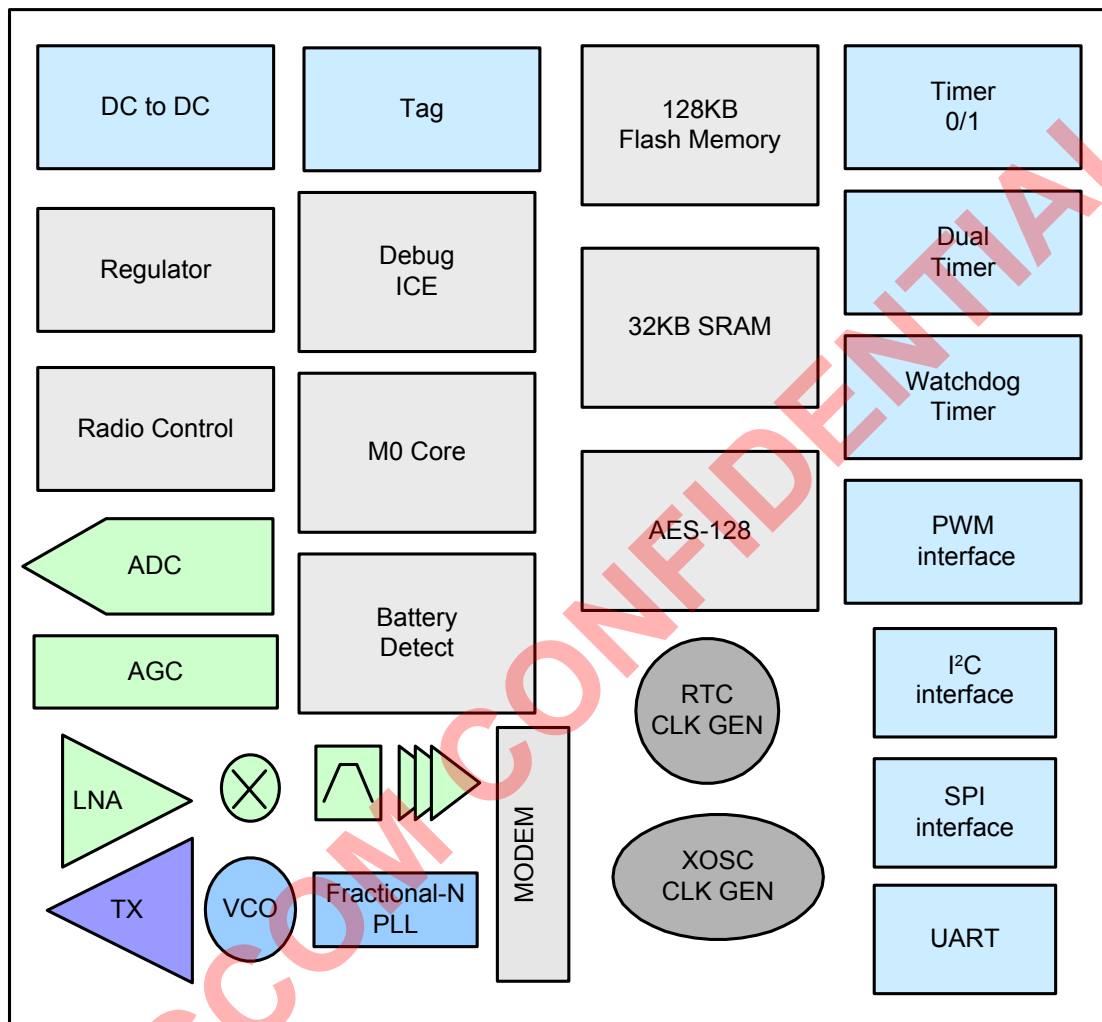


Figure 6.1 A8125M0 Block Diagram

7. Absolute Maximum Ratings

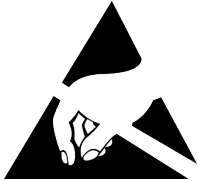
Parameter	With respect to	Rating	Unit
Supply voltage range (VDD_IO)	GND	-0.3 ~ 3.6	V
Digital IO pins range	GND	-0.3 ~ VDD_IO+0.3	V
Voltage on the analog pins range	GND	-0.3 ~ Core voltage+0.3	V
Input RF level		10	dBm
Storage Temperature range		-55 ~ 125	°C
ESD Rating	HBM	+/- 2KV*	V
	MM	+/- 100V*	V

*Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions. HBM (Human Body Mode) is tested under MIL-STD-883F Method 3015.7. MM (Machine Mode) is tested under JEDEC EIA/JESD22-A115-A.

*Device is Moisture Sensitivity Level III (MSL 3).

* RF PIN is HBM ± 1000V and MM ± 50V.



8. Electrical Specification

(Ta=25°C, VDD_IO=3.3V, data rate= 2Mbps, F_{XTAL} =16MHz, On Chip Regulator = 1.2V, PN9 pattern, with matching network and low pass filter, unless otherwise noted.)

Parameter	Description	Min.	Typ.	Max.	Unit
General					
Operating Temperature		-40		85	°C
Supply Voltage (VDD_IO)	VDD_IO supply input	2.0		3.6	V
Current Consumption (MCU in stop MODE, and RF in sleep MODE)	PM1 with sleep timer (1KB SRAM retention)		2.7		uA
	PM2 with sleep timer (1KB SRAM retention)		2.7		uA
	PM3 with sleep timer (1KB SRAM retention)		2		uA
	PM3 without sleep timer (1KB SRAM retention)		1.7		uA
	Deep sleep		0.5		uA
Current Consumption (MCU in normal MODE) Without DC-DC MCU Clock @16MHz	Sleep MODE		4		mA
	Standby MODE		4.6		mA
	PLL MODE		9.2		mA
	RX MODE (AGC On)		16.5		mA
	TX MODE (@5dBm output)		21.5		mA
	TX MODE (@10dBm output)		36		mA
Current Consumption (MCU in STOP MODE) Without DC-DC	Standby MODE		2		mA
	PLL MODE		6.7		mA
	RX MODE (AGC On)		14		mA
	TX MODE (@5dBm output)		19		mA
	TX MODE (@10dBm output)		33.5		mA
Current Consumption (MCU in STOP MODE) With DC-DC	Standby MODE		1.3		mA
	PLL MODE		3.7		mA
	RX MODE (AGC On)		7.1		mA
	TX MODE (@5dBm output)		9.2		mA
	TX MODE (@10dBm output)		24.5		mA
Synthesizer block					
Crystal settling time* ¹	PM to standby (XTAL SMD2016)		0.6		ms
Crystal frequency			16		MHz
Crystal tolerance* ²			±20		ppm
Crystal Load Capacitance			9		pF
Crystal ESR				80	ohm
PLL settling time	Standby to PLL		50		μS
Transmitter					
Carrier Frequency		2400		2500	MHz
Maximum Output Power			10		dBm
RF Power Control Range			40		dB
Out Band Spurious Emission	30MHz~1GHz			-36	dBm
	1GHz~12.75GHz			-30	dBm
	1.8GHz~ 1.9GHz			-47	dBm
	5.15GHz~ 5.3GHz			-47	dBm
Data rate		8K	500K	2M	bps

Frequency deviation	2Mbps		500K		Hz
	1Mbps		250K		Hz
	500Kbps		125K		Hz
TX settling time	Standby to TX		60		μs
Receiver					
Receiver sensitivity @ BER = 0.1%	2Mbps ($F_{IF} = 2\text{MHz}$)		-90		dBm
	1Mbps ($F_{IF} = 1\text{MHz}$)		-93		dBm
	500Kbps ($F_{IF} = 500\text{KHz}$)		-96		dBm
IF frequency bandwidth	2Mbps		2.5M		Hz
	1Mbps		1.25M		Hz
	500Kbps		625K		Hz
IF center frequency	2Mbps		2M		Hz
	1Mbps		1M		Hz
	500Kbps		500K		Hz
Interference* ³	Co-Channel (C/I_0)		11		dB
	1 st Adjacent Channel (C/I_1)		2		dB
	2 nd Adjacent Channel (C/I_2)		-18		dB
	3 rd Adjacent Channel (C/I_3)		-28		dB
	Image (C/I_{IM})		-12		dB
Maximum Operating Input Power	@RF input (BER=0.1%)		-15		dBm
RX Spurious Emission	30MHz~1GHz			-52	dBm
	1GHz~12.75GHz			-47	dBm
RSSI Range with AGC turn on	@RF input	-100		-20	dBm
RX settling time	Standby to RX		60		μs
12Bit SAR ADC					
Reference voltage	VREF_AD= VDD_AD		1.8		V
Input voltage range		0		VREF_AD	V
Input capacitor			25		pF
Sampling frequency		15.625		125	KHz
ENOB			10		bit
INL			+/- 1		LSB
DNL			+/-1		LSB
Current consumption			500		μA
Regulator					
Regulator settling time			200		μs
Band-gap reference voltage			1.2		V
Regulator output voltage			1.2		V
Digital IO DC characteristics					
High Level Input Voltage (V_{IH})		0.8* VDD_IO		VDD_IO	V
Low Level Input Voltage (V_{IL})		0		0.2* VDD_IO	V
High Level Output Voltage (V_{OH})	@ $I_{OH} = -0.5\text{mA}$	VDD_IO -0.4		VDD_IO	V
Source current	@ $V_{OH} = 2.4\text{V}$		10		mA
Low Level Output Voltage (V_{OL})	@ $I_{OL} = 0.5\text{mA}$	0		0.4	V
Sink current	@ $V_{OL} = 0.4\text{V}$		5		mA
DC-DC Buck converter					
Input voltage range		2.0		3.6	V

Output voltage		1.3	1.4	2.0	V
Efficiency	@ 3.3V input, 100 ohm load		85		%
Maximum load current				50	mA
Tag					
Power					
Limiter voltage			5		V
Transmitter					
Modulation scheme	Load modulation OOK				
Coding	Manchester				
Date rate			106		Kbps
Receiver					
Modulation scheme	ASK 100%				
Coding	Modified Miller				
Date rate			106		Kbps

Note 1: Crystal settling time is depended on crystal package type, ESR and Cm.

Note 2: For low data rate application, crystal tolerance should be tightened. Please contact AMICCOM's FAE.

Note 3: The wanted signal is set above sensitivity level +3dB. The modulation data of wanted signal and interferer are PN9 and PN15, respectively. Channel spacing is one IF frequency.

9. Register List

A8125M0 contains Peripheral Register, RF Register and Power Control Register

9.1 RF control register start at Address[31:0]= 0x50001000

9.1.1 Reset Register (Address: 0x50001000)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RESET	FWPR	FRPR	FIFOR	BFCR			
R								
Reset	0	0	0	0	0			
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

RESET: Soft reset. (Write only)

[0]: No reset.

[1]: Soft reset this device. Auto clear when done.

FWPR: FIFO write point reset. (Write only)

[0]: No reset.

[1]: reset FIFO write pointer. Auto clear when done.

FRPR: FIFO read point reset. (Write only)

[0]: No reset.

[1]: reset FIFO read pointer. Auto clear when done.

FIFOR: FIFO data reset. (Write only)

[0]: No reset.

[1]: Reset FIFO Data to all zero. Auto clear when done.

BFCR: Back-off counter reset. (Write this register to 1 to issue reset command, then it is auto clear.)

[0]: No reset.

[1]: Reset Back-off counter to zero. Auto clear when done.

9.1.2 Strobe Command Register (Address: 0x50001004)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	STRB7	STRB6	STRB5	STRB4	STRB3	STRB2	STRB1	STRB0
R								
Reset	0	0	0	0	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								

R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

Use strobe command control RF state.

Strobe[7:4] = 4'b1000: Sleep mode.

Strobe[7:4] = 4'b1001: Reserved mode.

Strobe[7:4] = 4'b1010: Standby .

Strobe[7:4] = 4'b1011: PLL mode.

Strobe[7:4] = 4'b1100: RX mode.

Strobe[7:4] = 4'b1101: TX mode.

9.1.3 Mode Control Register (Address: 0x50001008)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	FIFOSS		AIF	DFCD	DFCRC	FMT	FMS	
R	FIFOSS		AIF	CD		FMT	FMS	
Reset	0		1	0	0	0	0	
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								LENS
R								
Reset								0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

FIFOSS: FIFO sequence order select.

[0]: LSB first.

[1]: MSB first.

AIF: Auto IF. Recommend AIF = [1].

[0]: Disable.

[1]: Enable.

RF LO frequency will auto offset one IF frequency whenever entering to RX mode.

DFCD (Data Filter by CD): The received packet will be filtered out.

[0]: Disable.

[1]: Enable.

CD: Carrier detector (Read only).

[0]: Input power below threshold.

[1]: Input power above threshold.

DFCRC: Filter RX packet with CRC check.

[0]: Disable.

[1]: Enable.

FMT: Reserved for internal usage only.

FMS: Direct/FIFO mode select.

[0]: Direct mode.

[1]: FIFO mode.

LENS: Length sequence order select.

[0]: LSB first.

[1]: MSB first.

9.1.4 Status Register (Address: 0x50001010)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								
R	CER	XER	PLLER	TRSR	TRER	RFSTATE2	RFSTATE1	RFSTATE0
Reset								
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R	FPEN			CSMAF	CCAF	FPF	FECF	CRCF
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

CER: Chip Status. (Read only)

[0]: Chip is disabled.

[1]: Chip is enabled.

XER: Xtal Status. (Read only)

[0]: Crystal oscillator is disabled.

[1]: Crystal oscillator is enabled.

PLLER: PLL Status. (Read only)

[0]: PLL is disabled.

[1]: PLL is enabled after PLL strobe command.

TRSR: TRX Status II. (Read only)

[0]: RX mode.

[1]: TX mode.

Serviceable when TRER=1 (TRX is enable).

TRER: TRX Status I. (Read only)

[0]: TRX is disabled.

[1]: TRX is enabled.

RFSTATE[2:0]: RF state flag.

RFSTATE[2:0] = 3'b000: Sleep mode.

RFSTATE[2:0] = 3'b001: Reserved mode.

RFSTATE[2:0] = 3'b010: standby mode.

RFSTATE[2:0] = 3'b011: PLL mode.

RFSTATE[2:0] = 3'b100: TX mode

RFSTATE[2:0] = 3'b101: RX mode

FPEN: Frame pending bit.

CSMAF: CSMA function flag.

[0]: CSMA pass.

[1]: CSMA Fail.

CCAF: CCA flag.

[0]: CCA pass.

[1]: CCA fail.

FPF: FIFO pointer flag

FECF: FEC flag. (Read only and updated for each valid packet.)

[0]: FEC pass.

[1]: FEC error.

CRCF: CRC flag. (Read only and updated for each valid packet.)

[0]: CRC pass.

[1]: CRC error.

9.1.5 RF interrupt Register (Address: 0x50001014)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	ISTRN						TWIS	FPFIS
R	INT	INTF			IST3	IST2	IST1	IST0
Reset	0						0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

ISTRN: Interrupt state reset. (write only). Recommend ISTRN = [0].

[1]: Reset interrupts sources. Auto clear when done.

TWIS : TX wake-up interrupt select.

[0]: Before Final TX.

[1]: After Final TX.

INT: Interrupt source state.

[0]: None.

[1]: Busy.

INTF: Interrupt flag.

INTF status is shown as the respective function as the below table.

IST[3:0]: Interrupt source select.

IST[3:0]	Interrupt source	INTF (Bit 0)	Note
0000	none	none	
0001	WTR	CRCF	
0010	CSMA_CA	CSMAF	
0011	CCA	CCAF	
0100	ART	Reserved	
0101	EDM	None	
0110	FPFINT	FPF	
0111	ADCM	None	
1000	WOR	CRCF	
1001	TWOR	None	
1010	WOT	None	

9.1.6 ID I Register (Address: 0x50001018)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Reset	0	0	0	0	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
R	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
Reset	0	0	0	0	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16
R	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16
Reset	0	0	0	0	0	0	0	0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W	ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24
R	ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24
Reset	0	0	0	0	0	0	0	0

9.1.7 ID II Register (Address: 0x5000101C)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	ID39	ID38	ID37	ID36	ID35	ID34	ID33	ID32
R	ID39	ID38	ID37	ID36	ID35	ID34	ID33	ID32
Reset	0	0	0	0	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40
R	ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40
Reset	0	0	0	0	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	ID55	ID54	ID53	ID52	ID51	ID50	ID49	ID48
R	ID55	ID54	ID53	ID52	ID51	ID50	ID49	ID48
Reset	0	0	0	0	0	0	0	0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W	ID63	ID62	ID61	ID60	ID59	ID58	ID57	ID56
R	ID63	ID62	ID61	ID60	ID59	ID58	ID57	ID56
Reset	0	0	0	0	0	0	0	0

ID: Serial Packet ID (SID).

9.1.8 FIFO Control Register (Address: 0x50001020)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PHR7	PHR6	PHR5	PHR4	PHR3	PHR2	PHR1	PHR0
R	PHR7	PHR6	PHR5	PHR4	PHR3	PHR2	PHR1	PHR0
Reset	0	0	0	0	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W	FPM1	FPM0						
R	FPM1	FPM0						
Reset	0	0						

PHR [7:0]: Physical Header of IEEE 802.15.4.

It contains length of frame.

Write: TX FIFO Length.

Read: RX FIFO received length.

Payload length is programmable by PHR [7:0]. The physical FIFO depth is 64 bytes. A8125M0 also supports logical FIFO extension up to 256 bytes. The FIFO pointer margin for FIFO extension is 32 bytes.

FPM [1:0]: Reserved.

9.1.9 Data Rate Register (Address: 0x50001024)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
R	SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
Reset	0	0	0	0	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

SDR [7:0]: Data Rate Setting. On-air Data rate = MDR / (SDR+1).

MDR: Main data rate, please reference RF CK Control I Register.

9.1.10 RF GIO Register (Address: 0x50001028)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W		GIO1I			GIO1S3	GIO1S2	GIO1S1	GIO1S0
R						P_GIO2	P_GIO1	P_CKO
Reset		0			0	0	1	1
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W		GIO2I			GIO2S3	GIO2S2	GIO2S1	GIO2S0
R								
Reset		0			0	0	0	1
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W		CKOI				CKOS2	CKOS1	CKOS0
R								
Reset		0				0	0	0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

GIO1I: GIO1 pin output signal invert.

[0]: Non-inverted output.

[1]: Inverted output.

GIO1S [3:0]: GIO1 pin function select.

GIO1S	TX state	RX state
[0000]	INT (Interrupt)	
[0001]	WTR (Wait until TX or RX finished)	
[0010]	Wake up signal	
[0011]	EOAC (end of access code)	FSYNC (frame sync)
[0100]	TME0 (TX modulation enable)	CD (carrier detect)
[0101]	Preamble Detect Output (PMD0)	
[0110]	RXD (Direct mode)	
[0111]	TXD (Direct mode)	
[1000]	PDN_RX	
[1001]	PDN_TX	
[1010]	PASW	
[1011]	VTB[0]	
[1100]	DMII	
[1101]	EOFF	
[1110]	FPF	
[1111]	CKE	

P_CKO/P_GIO1/P_GIO2: I/O state, can read out.

GIO2I: GIO2 pin output invert.

[0]: Non-inverted output.

[1]: Inverted output.

GIO2S [2:0]: GIO2 pin function select.

GIO2S	TX state	RX state
[0000]	INT	
[0001]	WTR (Wait until TX or RX finished)	
[0010]	Wake up signal	
[0011]	EOAC (end of access code)	FSYNC (frame sync)
[0100]	TME0 (TX modulation enable)	CD (carrier detect)
[0101]	Preamble Detect Output (PMD0)	
[0110]	RXD (Direct mode)	
[0111]	TXD (Direct mode)	
[1000]	PDN_RX	
[1001]	PDN_TX	

[1010]	PASW
[1011]	VTB[1]
[1100]	DMIQ
[1101]	EOFF
[1110]	FPF
[1111]	CKE

EOFF: EOP, EOVCB, EOFBC, EOADC, EOVC, EOVC, EORSSC, OKADC, EOAGC (Internal usage only).

CKOI: CKO pin output signal invert.

[0]: Non-inverted output.

[1]: Inverted output.

CKOS [2:0]: CKO pin output select.

[000]: INTF.

[001]: BDF (Low battery detection output).

[010]: XRDY.

[011]: SDO (4 wires SPI data output).

[100]: BBCK (4XDR).

[101]: RO frequency / 10.

[110]: RO frequency.

[111]: Data clock (2M or 250K).

9.1.11 Channel Register (Address: 0x500010C0)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
R	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
Reset	0	1	1	0	0	1	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

CHN [7:0]: RF Channel Number.

9.1.12 TX Control Register (Address: 0x50001100)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PPS	TCPS	DEVSUB	GDR	FS	TXDI	TMDE	TME
R								
Reset	0	0	0	0	0	0	1	1
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W						FPS2	FPS1	FPS0
R								
Reset						0	0	0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								

Reset								
-------	--	--	--	--	--	--	--	--

PPS: TX delay fit data select.

[0]: Fit preamble carrier.

[1]: Fit SID data.

TCPS: TX delay fit carrier or preamble select(turbo mode).

[0]: Fit TX carrier.

[1]: Fit preamble data.

DEVSUB: TX deviation scale.

[0]: 1x.

[1]: 0.9x.

GDR: Gaussian Filter Over-sampling Rate select.

[0]: BT= 1.4~0.6

[1]: BT= 0.7~0.55

FS: Gaussian Filter Select.

[0]: Disable.

[1]: Enable.

Note: Please contact AMICCOM FAE for using Gaussian Filter.

TXDI: TX data invert. Recommend TXDI = [0].

[0]: Non-invert.

[1]: Invert.

TMDE: TX Modulation Enable for VCO Modulation. Recommend TMDE = [1].

[0]: Disable.

[1]: Enable.

TME: TX modulation enable.

[0]: Disable.

[1]: Enable.

FPS[2:0]: GF parameter select.

GDR=0

FPS[2:0]	7	6	5	4	3	2	1	0
BT	1.4	1.3	1.2	1.1	0.75	0.7	0.65	0.6

GDR=1

FPS[2:0]	7	6	5	4	3	2	1	0
BT	0.7	0.65	0.6	0.55	0.7	0.65	0.6	0.55

9.1.13 TX Power Register (Address: 0x50001104)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PWORS	TXCS	PAC2	PAC1	PAC0	TBG2	TBG1	TBG0
R								
Reset	0	0	0	0	0	1	1	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	VBPAS	IBPAS		PAV2	PAV1	PAV0	PAB_HCS	PA_HCS
R								
Reset	0	0		0	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	LTPA2	LTPA1	LTPA0	LTBG2	LTBG1	LTBG0	PDN_LPWRN	PDN_TXSW
R								
Reset	0	0	0	0	0	0	0	0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								

Reset								
-------	--	--	--	--	--	--	--	--

PWORS: Reserved for internal usage only.

TXCS: TX current select.

PAC [2:0]: PA Current Setting.

TBG [2:0]: TX Buffer Current Setting.

PAV [2:0]: PA voltage.

[000]: 1.2V.

[001]: 1.3V.

[010]: 1.4V.

[011]: 1.5V.

[100]: 1.6V.

[101]: 1.8V.

[110]: 1.9V.

[111]: 2.0V.

PA_HCS, PAB_HCS: Reserved for internal usage only.

IBPAS, VBPAS: PA power control. Reserved for internal usage only.

PDN_TXSW: TX switch control pin.

[0]: TX switch off

[1]: TX switch on

PDN_LPWRN: TX low power control pin.

[0]: TX low power

[1]: TX high power

LTBG[2:0]: TX Buffer current setting for low power.

LTPA[2:0]: PA current setting for low power.

9.1.14CODE I Register (Address: 0x50001180)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W					CRCIV	WHTS	FECS	CRCS
R								
Reset					0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W		ETH2	ETH1	ETH0	PTH2	PTH1	PTH0	IDL
R								
Reset		0	1	0	0	1	1	0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

CRCIV: CRC format invert.

[0]: Normal.

[1]: Invert.

WHTS: Data whitening (Data Encryption) select.

[0]: Disable.

[1]: Enable.

FECS: FEC select.

[0]: Disable.

[1]: Enable.

CRCS: CRC select.

[0]: Disable.

[1]: Enable.

ETH [2:0]: Received SID2 Code Error Tolerance. SID2 is only valid if ID length is 8bytes.

[000]: 0 bit.

[001]: 1 bit.

[010]: 2 bit.

[011]: 3 bit.

[100]: 4 bit.

[101]: 5 bit.

[110]: 6 bit.

[111]: 7 bit.

PTH [2:0]: Received SID1 Code Error Tolerance.

[000]: 0 bit.

[001]: 1 bit.

[010]: 2 bit.

[011]: 3 bit.

[100]: 4 bit.

[101]: 5 bit.

[110]: 6 bit.

[111]: 7 bit.

IDL: ID code length select.

[0]: 4 bytes.

[1]: 8 bytes.

9.1.15 CODE II Register (Address: 0x50001184)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W		WS6	WS5	WS4	WS3	WS2	WS1	WS0
R								
Reset		0	1	0	1	0	1	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								WHT9S
R								
Reset								0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

WS [6:0]: Data Whitening seed setting (data encryption key).

WHT9S: Data whitening 9 (Data Encryption) select.

[0]: Disable.

[1]: Enable.

9.1.16 CODE III Register (Address: 0x50001188)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CRCPL7	CRCPL6	CRCPL5	CRCPL4	CRCPL3	CRCPL2	CRCPL1	CRCPL0
R								
Reset	0	0	1	0	0	0	0	1
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	CRCPL15	CRCPL14	CRCPL13	CRCPL12	CRCPL11	CRCPL10	CRCPL9	CRCPL8
R								
Reset	0	0	0	1	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W							CRCM	CRC8S
R								
Reset							0	0

CRCPL[15:0]: CRC polynomial value.

CRC8S: CRC-8 select.

[0]: Disable.

[1]: Enable.

CRCM: Data comparing to CRC result.

[0]: 0.

[1]: Received CRC field.

9.1.17 CODE IV Register (Address: 0x5000118C)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CRCRIV7	CRCRIV6	CRCRIV5	CRCRIV4	CRCRIV3	CRCRIV2	CRCRIV1	CRCRIV0
R								
Reset	0	0	0	0	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	CRCRIV15	CRCRIV14	CRCRIV13	CRCRIV12	CRCRIV11	CRCRIV10	CRCRIV9	CRCRIV8
R								
Reset	0	0	0	0	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	CRCTIV7	CRCTIV6	CRCTIV5	CRCTIV4	CRCTIV3	CRCTIV2	CRCTIV1	CRCTIV0
R								
Reset	0	0	0	0	0	0	0	0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W	CRCTIV15	CRCTIV14	CRCTIV13	CRCTIV12	CRCTIV11	CRCTIV10	CRCTIV9	CRCTIV8
R								
Reset	0	0	0	0	0	0	0	0

CRCRIV[15:0]: CRC RX initial value.

CRCTIV[15:0]: CRC TX initial value.

9.1.18 RF TEST I Register (Address: 0x500011D4)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W			CSXTL5	CSXTL4	CSXTL3	CSXTL2	CSXTL1	CSXTL0
R								
Reset			0	1	1	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

W								
R								
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

CSXTL[5:0]: On-chip capacitor added on XI, XO pin, respectively.

CSXTL is the on-chip capacitor for XTAL oscillator to fine tune offset frequency of the wanted **RF** carrier.
The capacitance= (CSXTL [5:0]*0.365) pF.

9.1.19WOR/WOT I Register (Address: 0x50001200)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W				TWWS1		WORE	WOTE	TWWS
R						WORE	WOTE	
Reset				0		0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W			WUS1	WUS0	WTLP3	WTLP2	WTLP1	WTLP0
R								
Reset			1	1	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W				RNTWUNF1				RNTWUNF
R				TWUNF1				TWUNF
Reset				0				0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

WORE: Wake On RX enable.

[0]: Disable.

[1]: Enable.

WOTE: Wake On TX enable.

[0]: Disable.

[1]: Enable.

TWWS: Wake On Timer enable.

[0]: Disable.

[1]: Enable.

WUS [1:0]: Wake up select when WOR is enabled.

[00]: Detect carrier.

[01]: Detect IEEE 802.15.4 Sync word.

[10]: Detect IEEE 802.14.4 Beacon.

[11]: CRC pass.

WTLP[3:0]: WOT loop time.

RNTWUNF: Reset TWUN flag.

TWUNF: TWUN flag.

TWWS1: Wake On Timer1 enable.

[0]: Disable.

[1]: Enable.

RNTWUNF1: Reset TWUN1 flag.

TWUNF1: TWUN1 flag.

9.1.20 WOR/WOT II Register (Address: 0x50001204)

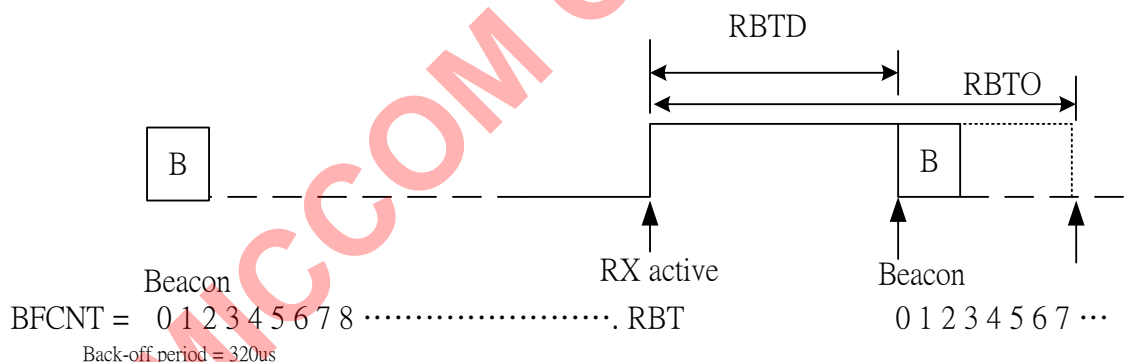
R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RBTO7	RBTO6	RBTO5	RBTO4	RBTO3	RBTO2	RBTO1	RBTO0
R	RBTD7	RBTD6	RBTD5	RBTD4	RBTD3	RBTD2	RBTD1	RBTD0
Reset	0	0	0	0	1	0	1	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	RBTO15	RBTO14	RBTO13	RBTO12	RBTO11	RBTO10	RBTO9	RBTO8
R	RBTD15	RBTD14	RBTD13	RBTD12	RBTD11	RBTD10	RBTD9	RBTD8
Reset	0	0	0	0	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

RBTO [15:0]: Random back off time-out in RX.

Time-out = (RBTO+1) * (RO frequency / 10) us.

RBTD [15:0]: Random back off difference.

The difference is the value between the active position and the beacon position.



9.1.21 WOR/WOT III Register (Address: 0x50001208)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RBT7	RBT6	RBT5	RBT4	RBT3	RBT2	RBT1	RBT0
R	BFCNT7	BFCNT6	BFCNT5	BFCNT4	BFCNT3	BFCNT2	BFCNT1	BFCNT0
Reset	0	0	0	0	0	1	0	1
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	RBT15	RBT14	RBT13	RBT12	RBT11	RBT10	RBT9	RBT8
R	BFCNT15	BFCNT14	BFCNT13	BFCNT12	BFCNT11	BFCNT10	BFCNT9	BFCNT8
Reset	0	0	0	0	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	RBT23	RBT22	RBT21	RBT20	RBT19	RBT18	RBT17	RBT16
R	BFCNT23	BFCNT22	BFCNT21	BFCNT20	BFCNT19	BFCNT18	BFCNT17	BFCNT16
Reset	0	0	0	0	0	0	0	0

R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

RBT [23:0]: Random back off active position. (write only)

Active time = (RBT+1) * (RO frequency / 10) us.

BFCNT [23:0]: Random back off counter. (read only)

It could show the position after enable back-off counter or received the beacon frame.

Each back off period is (RO frequency / 10) us.

Use the **BFCNT** to calculate the active position (**RBT**).

9.1.22 WOR/WOT IV Register (Address: 0x5000120C)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RBT1_7	RBT1_6	RBT1_5	RBT1_4	RBT1_3	RBT1_2	RBT1_1	RBT1_0
R	BFCNT1_7	BFCNT1_6	BFCNT1_5	BFCNT1_4	BFCNT1_3	BFCNT1_2	BFCNT1_1	BFCNT1_0
Reset	0	0	0	0	0	1	0	1
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	RBT1_15	RBT1_14	RBT1_13	RBT1_12	RBT1_11	RBT1_10	RBT1_9	RBT1_8
R	BFCNT1_15	BFCNT1_14	BFCNT1_13	BFCNT1_12	BFCNT1_11	BFCNT1_10	BFCNT1_9	BFCNT1_8
Reset	0	0	0	0	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	RBT1_23	RBT1_22	RBT1_21	RBT1_20	RBT1_19	RBT1_18	RBT1_17	RBT1_16
R	BFCNT1_23	BFCNT1_22	BFCNT1_21	BFCNT1_20	BFCNT1_19	BFCNT1_18	BFCNT1_17	BFCNT1_16
Reset	0	0	0	0	0	0	0	0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

RBT1 [23:0]: Random back off active position. (write only)

Active time = (RBT1+1) * (RO frequency / 10) us.

BFCNT1 [23:0]: Random back off counter. (read only)

It could show the position after enable back-off counter or received the beacon frame.

Each back off period is (RO frequency / 10) us.

Use the **BFCNT1** to calculate the active position (**RBT1**).

9.1.23 8BIT ADC Control Register (Address: 0x50001240)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	ADCC	ADCOM1	ADCOM0	AVGS1	AVGS0	ARSSI	CDM	ADCM
R	ADCC	ADCOM1	ADCOM0	AVGS1	AVGS0	ARSSI	CDM	ADCM
Reset	0	1	0	1	1	1	1	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

ADCC: ADC calibration (Auto clear when done).

[0]: Disable.

[1]: Enable.

ADCOM: ADC output mode.

[00]: Single mode.

[01]: ED average mode (2, 4, 8, 16 average is according to AVGS [1:0]).

[10]: Reserved.

[11]: ED. Hold after sync 128us.

AVGS [1:0]: ADC average mode. Recommend AVGS = [11].

[00]: 2.

[01]: 4.

[10]: 8.

[11]: 16.

ARSSI: Auto RSSI measurement whenever in RX mode. Recommend ARSSI = [1].

[0]: Disable.

[1]: Enable.

CDM: CD margin = CDTH – CDTL. Recommend CDM = [1].

[0]: 6 LSB.

[1]: 12 LSB.

ADCM: ADC measurement (Auto clear when done).

[0]: Disable.

[1]: Enable.

ADCM	Standby mode	RX mode
[0]	Disable ADC	Disable ADC
[1]	Measure temperature or external voltage	Measure RSSI, carrier detect

9.1.24 8Bit ADC Threshold Register (Address: 0x50001244)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CDTH7	CDTH6	CDTH5	CDTH4	CDTH3	CDTH2	CDTH1	CDTH0
R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
Reset	0	1	1	0	0	1	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

CDTH [7:0]: Carrier detect threshold (write only).

ADC [7:0]: ADC digital output value (read only).

ADC input voltage = 0.6 * ADC [7:0] / 256 V.

9.1.25 8Bit ADC CAL Register (Address: 0x50001248)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	MRHL	RSSL6	RSSL5	RSSL4	RSSL3	RSSL2	RSSL1	RSSL0
R	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
Reset	0	0	0	1	1	0	0	1

R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W			CRS2	CRS1	CRS0	SRS2	SRS1	SRS0
R	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0
Reset			1	0	0	1	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R	ADL7	ADL6	ADL5	ADL4	ADL3	ADL2	ADL1	ADL0
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R	ADH7	ADH6	ADH5	ADH4	ADH3	ADH2	ADH1	ADH0
Reset								

MRHL: AGC Manual scale select. Recommend MRHL = [0].

[0]: By (RL–RH).

[1]: By RSSL[6:0].

RSSL[4:0]: AGC Manual Scale setting. Recommend RSSL = [00000].

RL [7:0]: RSSI Calibration Low Threshold (read only).

RH [7:0]: RSSI Calibration High Threshold (read only).

CRS, SRS: RSSI Calibration parameter. Reserved for internal usage.

ADL[7:0]: AD low level calibration result.

ADH[7:0]: AD high level calibration result.

9.1.26 RF4CE Mode Select Register (Address: 0x50001300)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CCAS		LQIS	ACKS	ARTS	CSMAS	SLOT	DLS
R	CCAS							
Reset	0		1	1	0	1	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	FMSS						ERX	EDS
R								EDS
Reset	0						0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W				CCAM1	CCAM0	SLT2	SLT1	SLT0
R								
Reset				0	1	0	0	0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W	TDLS							
R								
Reset	0							

CCAS: CCA function. (Auto clear when done).

[0]: Disable.

[1]: Enable.

LQIS: LQI Select. Recommend LQIS = [1].

[0]: Disable.

[1]: Enable.

ACKS: Auto ACK enable.

[0]: Disable.

[1]: Enable.

ARTS: Auto Resend enable.

[0]: Disable.

[1]: Enable.

CSMAS: CSMA-CA enable.

[0]: Disable.

[1]: Enable.

SLOT: CSMA_CA algorithm type.

[0]: Un-slotted.

[1]: Slotted.

DLS: Dynamic length select.

[0]: deselect.

[1]: select.

FMSS: FMS select for EDS/CCA.

[0]: Normal FMS.

[1]: For CCA and ED. When CCA or ED active, FMS = 0.

ERX: RX Behavior.

[0]: Normal RX.

[1]: For CCA and ED. When CCA or ED is done, auto back to previous state (i.e. Standby or PLL mode).

EDS: Energy detect. (Auto clear when done).

[0]: Disable.

[1]: Enable.

CCAM[1:0]: CCA mode. Recommend CCAM = [01].

[00]: CCAF=1, when RSSI > RTH, and detect preamble frame.

[01]: CCAF=1, when RSSI > RTH.

[10]: CCAF=1, when detect preamble frame.

[11]: CCAF=1, when RSSI > RTH or detect preamble frame.

SLT[2:0]: TRX lead time in slotted mode.

[000]: 2 slot time.

[001]: 3 slot time.

[010]: 4 slot time.

[011]: 5 slot time.

[100]: 6 slot time.

[101]: 7 slot time.

[110]: 8 slot time.

[111]: 9 slot time.

TDLS: T Type Dynamic length select.

[0]: deselect.

[1]: select.

9.1.27 TX/RX FIFO Register (Address: 0x50001400h~0x500014FF)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx
R	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx
Reset	0	0	0	0	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx
R	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx
Reset	0	0	0	0	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx
R	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx
Reset	0	0	0	0	0	0	0	0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx
R	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx	FIFOx
Reset	0	0	0	0	0	0	0	0

The physical FIFO depth is 64 bytes. A8125M0 also supports logical FIFO extension up to 256 bytes.

9.1.28 USID Register (Address: 0x5000F000)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								
R	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
Reset								
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R	DID23	DID22	DID21	DID20	DID19	DID18	DID17	DID16
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R	DID31	DID30	DID29	DID28	DID27	DID26	DID25	DID24
Reset								

DID [31:0]: 0x01812507

9.2 Power control register start at Address[31:0]= 0x50000000

9.2.1 Battery detect Register (Address: 0x50000000)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W				BLE	BDV2	BDV1	BDV0	BDE
R					BDV2	BDV1	BDV0	BDF
Reset				0	0	0	1	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

BLE: Battery life extension. Reserved for internal usage.

BDV[2:0]: Battery detection voltage.

[000]: 2.0V.

[001]: 2.1V.

[010]: 2.2V.

[011]: 2.3V.

[100]: 2.4V.

[101]: 2.5V.

[110]: 2.6V.

[111]: 2.7V.

BDE: Battery detection enable.

[0]: Disable.

[1]: Enable.

BDF: Battery detection flag.

[0]: Low Battery.

[1]: High Battery.

9.2.2 Flash Control Register (Address: 0x50000004)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PDNFL2	QDSFL2	PDNFL1	QDSFL1	PDNFH	QDSFH	PDNFL	QDSFL
R								
Reset	1	0	1	0	1	0	1	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W				AUTO	PDNFL4	QDSFL4	PDNFL3	QDSFL3
R								
Reset				1	1	0	1	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								

R								
Reset								

PDNFH, QDSFH, PDNFL, QDSFL: Flash power control at PM mode.

PDNFL1, QDSFL1: SRAM (1KB ~ 4KB) power control at PM mode.

PDNFL2, QDSFL2: Reserved.

PDNFL3, QDSFL3: PWM power control at PM mode.

PDNFL4, QDSFL4: SRAM (4KB ~ 32KB) power control at PM mode.

AUTO: Auto mode of flash pumping circuit.

9.2.3 Power Control I Register (Address: 0x50000008)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PDNDS	PMVSDS	PWMS	PM1S	QD	REGAE	PM3S	STOP
R			PWMS	PM1S	QD	REGAE	PM3S	STOP
Reset	0	1		0	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	PM1SW1	PM1SW0	CPPSN	PMPAR	CLKSEL2	CLKSEL1	CLKSEL0	PMM
R					CLKSEL2	CLKSEL1	CLKSEL0	PMM
Reset	0	0	1	1	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	PD_LVD	RNBOD	PMVSAD	PMVSPA	PMVSP	CLR	CLR	CLR
R						BODF	RESETNF	PORF
Reset	0	0	0	0	0	0	0	0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W	BODS	PM1SWE	STDLY1	STDLY0	PDNADS	PSD2	PSD1	PSD0
R								
Reset	0	0	0	0	0	0	0	1

PDNDS,PMVSDS:PDND/PMVSD control select.(reset value: PDNDS=0,PMVSDS=1)

	PDNDS=0 ; PDNDS=1		PMVSDS=0 ; PMVSDS=1	
	PDND		PMVSD	
Normal	1	1	0	0
PM1	0	1	0	1
PM2	0	1	0	1
PM3	0	0	0	0

PWMS: PMW IO function select

[0]: Deselect.

[1]: Select.

PM1S: Power Mode 1 select

[0]: Deselect.

[1]: Select.

QD: Quick discharge Enable

[0]: Disable

[1]: Enable

REGAE: RegA Enable

[0]: Disable

[1]: Enable

PM3S: Power Mode 3 select

[0]: Deselect.

[1]: Select.

STOP: Stop mode

[0]: Disable

[1]: Enable

PM1SWE, PM1SW[1:0],CPPSN,PMPAR.(for PM mode control)

CLKSEL[2:0] (Clock Select), Select clock source when enable clock select.

[000]: Clock source div 64 as MCU clock

[001]: Clock source div 2 as MCU clock

[010]: Clock source div 4 as MCU clock

[011]: Clock source div 8 as MCU clock

[100]: Clock source div 16 as MCU clock

[101]: Clock source div 32 as MCU clock

[110]: Clock source div 64 as MCU clock

[111]: Select RTC as CPU clock when CKSE=0; RTC div 2 as CPU clock when CKSE=1

PMM: Power management mode

[0]: Disable

[1]: Enable

PD_LVD: LVD circuit power down.

When PD_LVD=0 and VDD_IO voltage less than 1.8v, the LVD circuit will generate a low voltage reset signal.

[0]: Power on.

[1]: Power down.

CLR: Clear flag

[0]: No clear.

[1]: Clear flag.

BODF: Low voltage detect flag

[0]: No low voltage reset.

[1]: Low voltage reset occurred.

RESETNF: Resetrn flag

[0]: No RESETN reset.

[1]: RESETN reset occurred.

PORF: Power-on reset flag

[0]: No POR reset.

[1]: POR reset occurred.

BODS: BOD flag select

STDLY[1:0]: Soft start delay.

PSD[2:0]: power saving wake-up delay. Reserved for internal usage.

RNBOD: Reserved.

PMVSAD, PMVSPA, PMVSP: PM mode power switch enable.

[0]: Disable.

[1]: Enable.

PDNADS: PDNAD select.

[0]: PDNAD=0.

[1]: PDNAD=0 at PM; =1 at normal mode.

9.2.4 Power Control II Register (Address: 0x5000000C)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-----	-------	-------	-------	-------	-------	-------	-------	-------

W	REGCL	REGVS	CBG4	CBG3	CBG2	CBG1	CBG0	BGS
R								
Reset	0	0	1	0	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	ADV0	STND	STNP	STNA	STNI	BGVRLS1	BGVRLS0	REGCS
R								
Reset	0	1	0	1	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								ADV1
R								
Reset								0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W	PORIPS				TCKS3	TCKS2	TCKS1	TCKS0
R								
Reset	0				0	0	0	0

BGS: Bangap (BG) select:

[0]: Low current BG.

[1]: High current BG.

CBG [4:0]: BG voltage adjust.

REGVS: Regulator voltage select. Reserved for internal usage.

REGCL: Low current regulator. Reserved for internal usage.

REGCS: Regulator current select. Reserved for internal usage.

BGVRLS[1:0]: Normal BG voltage select.

[00]: 1.2V.

[01]: 1.1V.

[10]: 1.0V.

[11]: 0.9V.

STND,STNP,STNA,STNI: Soft start for regulator D/P/A.PA

ADV [1:0]: AD voltage select.

TCKS [3:0]:Timer clock source select.

TCKS[0] for Timer0;

TCKS[1] for Timer1;

TCKS[2] for Dual Timer0;

TCKS[3] for Dual Timer1;

Command value:

[0]: 16M clock source.

[1]: 32K clock source.

PORIPS: Reserved.

9.2.5 DCDC Control 1 Register (Address: 0x50000014)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W		DCCBG2	DCCBG1	DCCBG0		RFAR2	RFAR1	RFAR0
R								
Reset		0	1	0		0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
Reset								

R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

DCCBG [2:0]: DC-DC BG voltage adjust.

RFAR [2]: Reserved.

RFAR [1:0]: DCDC auto mode select in PM.

[00]: Manual mode.

[01]: Auto to bypass mode.

[10]: Reserved.

[11]: Auto to sleep mode.

9.2.6 DCDC Control 2 Register (Address: 0x50000018)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	MS7	MS6	MS5	MS4	MS3	MS2	MS1	MS0
R								
Reset	0	0	0	0	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

MS [7:0]: DCDC mode select.

MS [7:0] = {PDNX, PDNA, MFC[2], PWMS, PDNBTL, DVT, STA, PDSY}.

[00X00000]: Bypass mode.

[10X00000]: Sleep mode.

[11X10001]: PWM mode.

Others: Reserved.

9.2.7 DCDC Control 3 Register (Address: 0x5000001C)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
R								
Reset	0	0	0	0	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								

R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

MR [7:0]: DCDC control.

MR [7:0]= {MDH [1:0], REG [3:0], MFC [1:0]}.

MDH [1:0]: Reserved.

REG [3:0]: DCDC output voltage select.

[0000]: 1.3V.

[0001]: 1.4V.

[0010]: 1.5V.

[0011]: 1.6V.

[0110]: 1.7V.

[0111]: 1.8V.

[10XX]: 1.25V.

[11XX]: 2.0V.

Others: Reserved.

MFC [2:0]: DCDC PMW frequency select.

[000]: 300KHz.

[001]: 750KHz.

[010]: 1.5MHz.

[011]: 1.8MHz.

[100]: 1.2MHz.

[101]: 2.0MHz.

[110]: 3.2MHz.

[111]: 3.5MHz.

9.2.8 HDV Register (Address: 0x50000020)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	HDV7	HDV6	HDV5	HDV4	HDV3	HDV2	HDV1	HDV0
R								
Reset	0	0	0	0	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	HDV15	HDV14	HDV13	HDV12	HDV11	HDV10	HDV9	HDV8
R								
Reset	0	0	0	0	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	HDV23	HDV22	HDV21	HDV20	HDV19	HDV18	HDV17	HDV16
R								
Reset	0	0	0	0	0	0	0	0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W	HDV31	HDV30	HDV29	HDV28	HDV27	HDV26	HDV25	HDV24
R								
Reset	0	0	0	0	0	0	0	0

HDV[31:0]: High driving setting for IOPAD.

9.2.9 IO Mode Control Register (Address: 0x50000024)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	WBUS7	WBUS6	WBUS5	WBUS4	WBUS3	WBUS2	WBUS1	WBUS0
R							PM4F	DSF
Reset	0	0	0	0	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	P3PLH	P2PLH	P1PLH	P0PLH	P3LH	P2LH	P1LH	P0LH
R								
Reset	0	0	0	0	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W							MFLH	MTLH
R								
Reset							0	0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

WBUS [7:0]: IO mode control write data bus.

WBUS [7:0] = PLSH3 [7:0] for P3PLH enable. (P3 is not used in A8125M0)

WBUS [7:0] = PLSH2 [7:0] for P2PLH enable.

WBUS [7:0] = PLSH1 [7:0] for P1PLH enable.

WBUS [7:0] = PLSH0 [7:0] for P0PLH enable.

WBUS [7:0] = DIEH3 [7:0] for P3LH enable. (P3 is not used in A8125M0)

WBUS [7:0] = DIEH2 [7:0] for P2LH enable.

WBUS [7:0] = DIEH1 [7:0] for P1LH enable.

WBUS [7:0] = DIEH0 [7:0] for P0LH enable.

WBUS [7:0] = MF [7:0] for MFLH enable.

WBUS [7:0] = MT [7:0] for MTLH enable.

MFLH, MTLH, P3LH, P2LH, P1LH, P0LH, P3PLH, P2PLH, P1PLH, P0PLH: IO mode data latch.

[0]: Disable.

[1]: Enable latch, auto clear.

PLSHx: IOPAD internal pull high low select.

[0]: Pull High

[1]: Pull low

DIEHx: Px input enable.

[0]: Tri-state

[1]: Enable

MF [7:0]= {PDNFC, MTPS, CKOS, DLS, MPRS, TP, RGC [1:0]}.

PDNFC: NFC enable.

[0]: Disable.

[1]: Enable.

MTPS: Reserved for internal use.

CKOS: NFC clock source select.

[0]: Recovery clock.

[1]: PLL clock.

DLS: NFC voltage limit adjust.

[0]: High.

[1]: Low.

MPRS: Reserved for internal use.

TP: Reserved for internal use.

RGC [1:0]: NFC BG current adjust.

MT [7:0]= {LCBG [2:0], LRGC [1:0], MT [2:0]}.

LCBG [2:0]: Low current BG voltage adjust.

LRGC [1:0]: Low current BG current adjust.

MT [2:0]: Deep sleep / PM4 mode select.

[xx0]: Deep sleep

[x01]: PM4

[x11]: Deselect

PM4F: PM4 mode flag.

[0]: Deselect

[1]: Select

DSF: Deep sleep flag.

[0]: Deselect

[1]: Select

9.2.10 RC Control I Register (Address: 0x50000040)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RCOT2	RCOT1	RCOT0	IRCHC	RTCS	ROE	RCKS1	RCKS0
R								
Reset	1	0	0	0	0	1	0	1
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	RC_MOD1	RC_MOD0		MAN	MCAL	RCMVS1	RCMVS0	ENCAL
R								ENCAL
Reset	0	0		0	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	MRCT7	MRCT6	MRCT5	MRCT4	MRCT3	MRCT2	MRCT1	MRCT0
R	RCT7	RCT6	RCT5	RCT4	RCT3	RCT2	RCT1	RCT0
Reset	0	0	0	0	0	0	0	0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W		MRFIN2	MRFIN1	MRFIN0			MRCT9	MRCT8
R		RFIN2	RFIN1	RFIN0			RCT9	RCT8
Reset		1	0	0			0	0

RCOT [2:0]: Reserved for internal usage only.

IRCHC: RC oscillator high current mode select.

RTCS: Sleep timer select.

[0]: RC oscillator (Internal).

[1]: RTC crystal oscillator (External).

ROE: Enable Internal RC oscillator.

[0]: Disable.

[1]: Enable.

RCKS [1:0]: RO calibration clock select:

[00]: 32XMDR
[01]: 16MHz
[10]: 8XMDR
[11]: 4XMDR

RC_MODE[1:0]: RC-OSC calibration mode select.

[00]: Auto-cal for RCOC[9:0].
[01]: Auto-cal for RCOC[9:0] and RFIN[2:0].
[10]: Auto/Manual-fine cal for RCOC[9:0] and RFIN[2:0].
[11]: Reserved.

MAN: RCOSC Manual calibration initial value setting select.

MCAL: Enable Continuous RC-OSC Calibration.

[0]: Continuous mode.
[1]: Single mode.

RCMVS[1:0]: RCOSC calibration moving average setting.

[00]: No average.
[01]: average 2 .
[10]: average 4.
[11]: average 8.

ENCAL: RC calibration enable.

[0]: Disable
[1]: Enable.

MRCT[9:0]: Manual RC calibration value setting

RCT [9:0]: RC-OSC calibration value.

MRFIN: RC-OSC fine tuned value manual setting.

RFIN: RC-OSC fine tuned value.

9.2.11 RC Control II Register (Address: 0x50000044)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	TGNUM7	TGNUM6	TGNUM5	TGNUM4	TGNUM3	TGNUM2	TGNUM1	TGNUM0
R	NUMLH7	NUMLH6	NUMLH5	NUMLH4	NUMLH3	NUMLH2	NUMLH1	NUMLH0
Reset	0	0	0	0	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W			TGNUM13	TGNUM12	TGNUM11	TGNUM10	TGNUM9	TGNUM8
R			NUMLH	NUMLH	NUMLH	NUMLH	NUMLH	NUMLH
Reset			0	0	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	RCIE	BIAS	CMP1	CMP0	IGM3	IGM2	IGM1	IGM0
R		SDINR6	SDINR5	SDINR4	SDINR3	SDINR2	SDINR1	SDINR0
Reset	0	0	0	0	0	0	0	0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W	RC_SIN	RC_SEL	MANS	--	MV_SEL1	MV_SEL0	MVS11	MVS10
R					SDINC3	SDINC2	SDINC1	SDINC0
Reset	0	0	0	0	0	0	0	1

TGNUM[13:0]: Target Number for RC OSC Calibration.

NUMLH[13:0]: RC-OSC calibration latch number.

RCIE: RC-OSC interrupt enable.

[0]: Disable.

[1]: Enable.

BIAS: Changes a bias of the comparator in IRC to save a current consumption.(Reserved for internal usage)

CMP[1:0]: Reduces frequency of IRC for 8 second application. (Reserved for internal usage)

IGM[3:0]: Adjusts current of the comparator in IRC. (Reserved for internal usage)

SDINR[6:0]: R difference. $SDINR[6:0] = DIFF[10:0] * (PAR2[6:0] + 1) * DIVR \text{ SCALE}$.

RC_SIN: RCOSC auto count single mode for RC_MODE=2.

RC_SEL: RCOSC auto calibration mode setting for RC_MODE=1.

MANS: RCOSC auto calibration initial value setting select for RC_MODE=1.

MV_SEL[1:0]: RCOSC calibration moving average setting.

[00]: No average.

[01]: average 2 .

[10]: average 4.

[11]: average 8.

MVS1[1:0]: RCOSC calibration delay setting. [00]: 4*RC clk. [01]: 8*RC clk [10]: 16*RC clock. [11]: 32*RC clock.

SDINC[3:0]: C difference. $SDINC[3:0] = DIFF[10:0] * (PAR1[3:0] + 1) * DIVC \text{ SCALE}$.

9.2.12 RC Target Control Register (Address: 0x50000048)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W					PAR1	PAR1	PAR1	PAR1
R	DIFFi7	DIFFi6	DIFFi5	DIFFi4	DIFFi3	DIFFi2	DIFFi1	DIFFi0
Reset					0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W		PAR2	PAR2	PAR2	PAR2	PAR2	PAR2	PAR2
R					DIFFi11	DIFFi10	DIFFi9	DIFFi8
Reset		0	0	0	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	SWM	DIV23	DIV21	DIV20		DIV13	DIV11	DIV10
R	DIFF7	DIFF6	DIFF5	DIFF4	DIFF3	DIFF2	DIFF1	DIFF0
Reset	0	0	0	0	0	0	0	0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W		RMR_SCAL6	RMR_SCAL5	RMR_SCAL4	RMR_SCAL3	RMR_SCAL2	RMR_SCAL1	RMR_SCAL0
R						DIFF10	DIFF9	DIFF8
Reset		1	0	0	0	0	0	0

PAR1[3:0]: C SCALE. $SDINC[3:0] = DIFF[10:0] * (PAR1[3:0] + 1) * DIVC \text{ SCALE}$.

DIFF[10:0]: RCOSC calibration counter difference(absolute values).

SWM: Selection of 32kHz oscillator. (Reserved for internal usage)

DIFF1[11:0]: RCOSC calibration counter difference.

PAR2[6:0] R SCALE. $SDINR[6:0] = DIFF[10:0] * (PAR2[6:0] + 1) * DIVR \text{ SCALE}$.

DIV1[2:0]: DIVC SCALE:

[000]: 1/8.

[001]: 1/16.

[010]: 1/32.

[011]: 1/64.

[100]: 1/64.

[101]: 1/128.

[110]: 1/256.

[111]: 1/512.

RMR_SCAL[6:0]: R scale for carry or borrow.

9.2.13 32K Crystal Inner Capacitance Load (Address: 0x5000004C)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W				RTCCL4	RTCCL3	RTCCL2	RTCCL1	RTCCL0
R								
Reset				1	1	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

RTCCL[4:0]: 32K crystal inner capacitance load $RTCCL \times 0.5pF$.

9.2.14 XRC Control I Register (Address: 0x50000050)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W			EKICR1	EKICR0	XRCS	ENRC	MXRC	XRCC
R								XRCC
Reset			0	0	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

EKICR[1:0]: Enable kick-off circuit select.

[00]: 0us;

[01]: 10us;

[1x]: 20us.

XRCS: Main clock source select.

[0]: Crystal oscillator (External). [1]: XRC oscillator (Internal)

ENRC: Enable Internal XRC oscillator.

[0]: Disable.

[1]: Enable.

MXRC: XRO bank manual calibration.

[0]: Disable.

[1]: Enable.

XRCC: XRO bank calibration (Auto clear when done).

[0]: Disable.

[1]: Enable.

9.2.15 XRC Control II Register (Address: 0x50000054)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	MTRIM7	MTRIM6	MTRIM5	MTRIM4	MTRIM3	MTRIM2	MTRIM1	MTRIM0
R	TRIM7	TRIM6	TRIM5	TRIM4	TRIM3	TRIM2	TRIM1	TRIM0
Reset	0	0	1	1	1	0	1	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								MTRIM8
R								TRIM8
Reset								1
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W					CI1	CI0	ICONTROL1	ICONTROL0
R								
Reset					1	0	1	0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W							MVXS1	MVXS0
R								
Reset							0	0

MTRIM [8:0]: XRO Bank manual calibration value (write only).

Manual setting when MXRC =1.

TRIM [8:0]: XRO Bank auto calibration value (read only).

CI[1:0]: Reserved for internal usage only.

ICONTROL[1:0]: Reserved for internal usage only.

MVXS [1:0]: XRO calibration moving average mode.

[00]: 1

[01]: 2

[10]: 4

[11]: 8

9.2.16 XRC Target Control Register (Address: 0x50000058)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	XTGNUM7	XTGNUM6	XTGNUM5	XTGNUM4	XTGNUM3	XTGNUM2	XTGNUM1	XTGNUM0
R	NUMLH7	NUMLH6	NUMLH5	NUMLH4	NUMLH3	NUMLH2	NUMLH1	NUMLH0
Reset	0	0	0	0	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W						XTGNUM10	XTGNUM9	XTGNUM8
R						NUMLH10	NUMLH9	NUMLH8
Reset						0	1	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

XTGNUM [10:0]: RO N Counter target (write only).

RO N Counter calibration goal or manual setting.

9.2.17 Wake Up Select Register(Address: 0x5000005C)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W							EDGTS1	EDGTS0
R							EDGTS1	EDGTS0
Reset							1	1
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

EDGTS[1:0]: Wake up select.

[00]: Both positive and negative edge.

[01]: PLSH= 0: Negative edge; PLSH= 1: Positive edge.

[10]: PLSH= 0: Positive edge; PLSH= 1: Negative edge.

[11]: Level.

9.3 12bit ADC control register start at Address[31:0]= 0x50008000

9.3.1 12bit ADC Control Register (Address: 0x50008000)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	BUFS12B			MODE12	MVS12B2	MVS12B1	MVS12B0	ADCE12
R				MODE12	MVS12B2	MVS12B1	MVS12B0	ADCE12
Reset	0			0	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	ADCIO3	ADCIO2	ADCIO1	ADCIO0			ADIVL	ADCYC
R								
Reset	0	0	0	0			0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W					CKS1	CKS0	DELS1	DELS0
R								
Reset					0	0	0	0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

BUFS12B: buffer select for 12bit ADC.

[0]: deselect

[1]: select.

MODE12: ADC 12bit mode.

[0]: one time.

[1]: continuous.

MVS12B [2:0]: 12bit ADC moving average mode.

[000]:1

[001]:2

[010]:3

[011]:4

[100]:5

[101]:6

[110]:7

[111]:8

ADCE12: ADC 12bit measurement enable.

[0]: disable

[1]: enable.

ADCIO[0]: ADC I/O enable

ADCIO[3:1]: ADC I/O select.

[000]: P0_18

[001]: P0_19

[002]: P0_08

[003]: P0_09

[004]: P0_12

[005]: P0_13

[006]: P0_14

[007]: P0_15

ADIVL: ADC 12bit initial value.

[0]:0

[1]:2048.

ADCYC: ADC 12bit counter reference.

[0]:31

[1]: 32

CKS[1:0]: ADC 12bit main clock select.

[00]:4M

[01]: 2M

[10]:1M

[11]: 0.5M

DELS[1:0]: ADC 12bit measurement delay select.

[00]:5us

[01]: 10us

[10]:15us

[11]: 20us.

9.3.2 12bit ADC Register (Address: 0x50008004)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								
R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
Reset								
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R					ADC11	ADC10	ADC9	ADC8
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

ADC12 [11:0]: ADC 12bit value.

9.3.3 12bit ADC INTSTATE Register (Address: 0x50008008)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								ADCI_Clear
R								ADCI_STATE
Reset								0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

ADCI_Clear: ADC 12bit INT clear.

[0]:normal

[1]:clear.

ADCI_STATE: ADC 12bit INT State.

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9.4AES128 control register start at Address[31:0]= 0x5000C0000

9.4.1 AES128 Control Register (Address: 0x5000C000)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W					KEYOS	AKFS	AESS	EDCRS
R								
Reset					0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
R								
Reset								
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R								
Reset								
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R								
Reset								

KEYOS: AES128 Key source read select.

[0]: If AKFS=1, from RX received encrypted AES128 key data.

If AKFS=0, from MCU write AES128 key data.

[1]: From encrypted/decrypted AES128 key data.

AKFS: Data packet with decrypted key appendixes select.

[0]: Disable.

[1]: Enable.

AESS: encryption format selection.

[0]: proprietary 32 bit.

[1]: Standard AES 128 bit.

EDCRS: Data encrypt or decrypt select.

[0]: Disable.

[1]: Enable.

9.4.2 AES128 KEY Register (Address: 0x5000C001h~0x5000C010)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY
R	KEYR	KEYR	KEYR	KEYR	KEYR	KEYR	KEYR	KEYR
Reset	0	0	0	0	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY
R	KEYR	KEYR	KEYR	KEYR	KEYR	KEYR	KEYR	KEYR
Reset	0	0	0	0	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY
R	KEYR	KEYR	KEYR	KEYR	KEYR	KEYR	KEYR	KEYR
Reset	0	0	0	0	0	0	0	0
R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY
R	KEYR	KEYR	KEYR	KEYR	KEYR	KEYR	KEYR	KEYR
Reset	0	0	0	0	0	0	0	0

KEY [127:0]: AES128 key input, total 16-bytes. (Write only).

KEYR [127:0]: AES128 key output, total 16-bytes. (Read only). Select by KEYOS.

9.5 Flash memory controller register start at Address[31:0]= 0x4001F000

Flash mode register (Offset: 0x100)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RBB	TRIM	-	INF	TM[3]	TM[2]	TM[1]	TM[0]
R								
Reset	1	0	0	0	0	0	0	0

RBB (Flash Ready status output)

[0]: Not Ready.

[1]: Ready

TRIM (Flash trim mode enable)

[0]: Disable

[1]: Enable

INF (Flash Information page enable)

[0]: Disable

[1]: Enable

TM[3:0] (Flash Test Mode enable)

Flash control register (Offset: 0x104)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CE			MERASE	SERASE	PERASE	PROG	WRONLY
R								
Reset	1	0	0	0	0	0	0	0

CE (Flash chip enable)

[0]: Disable

[1]: Enable

MERASE (Flash Mass Erase enable)

[0]: Disable

[1]: Enable

SERASE (Flash Sector Erase enable)

[0]: Disable

[1]: Enable

PERASE (Flash Page Erase enable)

[0]: Disable

[1]: Enable

PROG (Flash Page Program internal Erase and Write enable)

[0]: Disable

[1]: Enable

WRONLY (Flash Page Write enable)

[0]: Disable

[1]: Enable

Flash pwe register (Offset: 0x108)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PWE		PWE_ L[5]	PWE_ L[4]	PWE_ L[3]	PWE_ L[2]	PWE_ L[1]	PWE_ L[0]
R								
Reset	0	0	0	0	0	0	0	0

PWE (Flash IAP program enable)

[0]: Disable

[1]: Enable

PWE_L[5:0](Flash IAP program length)

[000001]: 1 double word.

[000010]: 2 double word.

...

[100000]: 32 double word.

Flash pwe start address register

Offset: 0x10C

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PWE_ A[7]	PWE_ A[6]	PWE_ A[5]	PWE_ A[4]	PWE_ A[3]	PWE_ A[2]	PWE_ A[1]	PWE_ A[0]
R								
Reset	0	0	0	0	0	0	0	0

Offset: 0x10D

R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	PWE_ A[15]	PWE_ A[14]	PWE_ A[13]	PWE_ A[12]	PWE_ A[11]	PWE_ A[10]	PWE_ A[9]	PWE_ A[8]
R								
Reset	0	0	0	0	0	0	0	0

Offset: 0x10E

R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	PWE_ A[23]	PWE_ A[22]	PWE_ A[21]	PWE_ A[20]	PWE_ A[19]	PWE_ A[18]	PWE_ A[17]	PWE_ A[16]
R								
Reset	0	0	0	0	0	0	0	0

Offset: 0x10F

R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W	PWE_ A[31]	PWE_ A[30]	PWE_ A[29]	PWE_ A[28]	PWE_ A[27]	PWE_ A[26]	PWE_ A[25]	PWE_ A[24]
R								
Reset	0	0	0	0	0	0	0	0

PWE_A[31:0](Flash IAP program start address)

Flash pwe program data register

Offset: 0x200

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PWE_ D0[7]	PWE_ D0[6]	PWE_ D0[5]	PWE_ D0[4]	PWE_ D0[3]	PWE_ D0[2]	PWE_ D0[1]	PWE_ D0[0]
R								
Reset	0	0	0	0	0	0	0	0

Offset: 0x201

R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	PWE_ D0[15]	PWE_ D0[14]	PWE_ D0[13]	PWE_ D0[12]	PWE_ D0[11]	PWE_ D0[10]	PWE_ D0[9]	PWE_ D0[8]
R								

R	D0[15]	D0[14]	D0[13]	D0[12]	D0[11]	D0[10]	D0[9]	D0[8]
Reset	0	0	0	0	0	0	0	0

Offset: 0x202

R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_
R	D0[23]	D0[22]	D0[21]	D0[20]	D0[19]	D0[18]	D0[17]	D0[16]
Reset	0	0	0	0	0	0	0	0

Offset: 0x203

R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_
R	D0[31]	D0[30]	D0[29]	D0[28]	D0[27]	D0[26]	D0[25]	D0[24]
Reset	0	0	0	0	0	0	0	0

Offset: 0x204

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_
R	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]
Reset	0	0	0	0	0	0	0	0

Offset: 0x205

R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_
R	D1[15]	D1[14]	D1[13]	D1[12]	D1[11]	D1[10]	D1[9]	D1[8]
Reset	0	0	0	0	0	0	0	0

Offset: 0x206

R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_
R	D1[23]	D1[22]	D1[21]	D1[20]	D1[19]	D1[18]	D1[17]	D1[16]
Reset	0	0	0	0	0	0	0	0

Offset: 0x207

R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_
R	D1[31]	D1[30]	D1[29]	D1[28]	D1[27]	D1[26]	D1[25]	D1[24]
Reset	0	0	0	0	0	0	0	0

Offset: 0x208

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_
R	D2[7]	D2[6]	D2[5]	D2[4]	D2[3]	D2[2]	D2[1]	D2[0]
Reset	0	0	0	0	0	0	0	0

Offset: 0x209

R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_	PWE_
R	D2[15]	D2[14]	D2[13]	D2[12]	D2[11]	D2[10]	D2[9]	D2[8]
Reset	0	0	0	0	0	0	0	0

Offset: 0x20A

R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	PWE_ D2[23]	PWE_ D2[22]	PWE_ D2[21]	PWE_ D2[20]	PWE_ D2[19]	PWE_ D2[18]	PWE_ D2[17]	PWE_ D2[16]
R								
Reset	0	0	0	0	0	0	0	0

Offset: 0x20B

R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W	PWE_ D2[31]	PWE_ D2[30]	PWE_ D2[29]	PWE_ D2[28]	PWE_ D2[27]	PWE_ D2[26]	PWE_ D2[25]	PWE_ D2[24]
R								
Reset	0	0	0	0	0	0	0	0

Offset: 0x27C

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PWE_ D1F[7]	PWE_ D1F[6]	PWE_ D1F[5]	PWE_ D1F[4]	PWE_ D1F[3]	PWE_ D1F[2]	PWE_ D1F[1]	PWE_ D1F[0]
R								
Reset	0	0	0	0	0	0	0	0

Offset: 0x27D

R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	PWE_ D1F[15]	PWE_ D1F[14]	PWE_ D1F[13]	PWE_ D1F[12]	PWE_ D1F[11]	PWE_ D1F[10]	PWE_ D1F[9]	PWE_ D1F[8]
R								
Reset	0	0	0	0	0	0	0	0

Offset: 0x27E

R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	PWE_ D1F[23]	PWE_ D1F[22]	PWE_ D1F[21]	PWE_ D1F[20]	PWE_ D1F[19]	PWE_ D1F[18]	PWE_ D1F[17]	PWE_ D1F[16]
R								
Reset	0	0	0	0	0	0	0	0

Offset: 0x27F

R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W	PWE_ D1F[31]	PWE_ D1F[30]	PWE_ D1F[29]	PWE_ D1F[28]	PWE_ D1F[27]	PWE_ D1F[26]	PWE_ D1F[25]	PWE_ D1F[24]
R								
Reset	0	0	0	0	0	0	0	0

PWE_D0[31:0](Flash IAP program data of start address)

PWE_D1[31:0](Flash IAP program data of start address+1)

PWE_D2[31:0](Flash IAP program data of start address+2)

...

PWE_D1F[31:0](Flash IAP program data of start address+32)

10. A8125M0 RF

A8125M0 integrate 2.4 GHz GFSK transceiver and use Strobe control register to control RF state. There are 6 Strobe commands to control internal state machine for RF operations. These MODEs include Sleep MODE, Reserved MODE, Standby MODE, PLL MODE, RX MODE and TX MODE. The physical FIFO depth is 64 bytes and it can supports logical FIFO extension up to 256 bytes. Sleep timer is used for WOR (Wake On Rx) and time-slotted MODE operation.

10.1 Strobe Command

Use strobe command control RF state and user can read the RF state from MODE register

10.1.1 Strobe Command - Sleep MODE

Refer to Strobe Control Register, user can write 0x80 to Strobe Control Register directly to set RF into Sleep MODE.

10.1.2 Strobe Command - Reserved MODE

Refer to Strobe Control Register, user can write 0x90 to Strobe Control Register directly to set RF into Reserved MODE.

10.1.3 Strobe Command - Standby MODE

Refer to Strobe Control Register, user can write 0xA0 to Strobe Control Register directly to set RF into Standby MODE.

10.1.4 Strobe Command - PLL MODE

Refer to Strobe Control Register, user can write 0xB0 to Strobe Control Register directly to set RF into PLL MODE.

10.1.5 Strobe Command - RX MODE

Refer to Strobe Control Register, user can write 0xC0 to Strobe Control Register directly to set RF into RX MODE.

10.1.6 Strobe Command - TX MODE

Refer to Strobe Control Register, user can write 0xD0 to Strobe Control Register directly to set RF into TX MODE.

10.2 RF Reset Command

In addition to power on reset (POR), A8125M0 could issue software reset to RF by setting RESET Register. A8125M0 generates an internal signal "RESETN" to initial RF circuit. After reset command, RF state is in standby MODE and re-calibration is necessary.

10.3 FIFO Accessing Command

Before TX delivery, user only needs to write wanted data into TX FIFO in advance. Similarly, user can read RX FIFO once payload data is received. It is easy to delivery data to air. Below is the procedure of writing TX FIFO.

Step1: Send (n+1) bytes TX data in sequence by Data Byte 0, 1, 2 to n.

Step2: Send TX Strobe command for transmitting.

There are similar steps to read RX FIFO.

Step1: Send RX Strobe command for receiving data.

Step2: Read RX data from RX FIFO in sequence by Data Byte 0, 1, 2 to n.

To use A8125M0's FIFO MODE, user just needs to enable FMS =1. For FIFO accessing, TX FIFO (write-only) and RX FIFO (read-only) share the same register address. TX FIFO represents transmitted payload. On the other hand, RX circuitry synchronizes ID Code and stores received payload into RX FIFO.

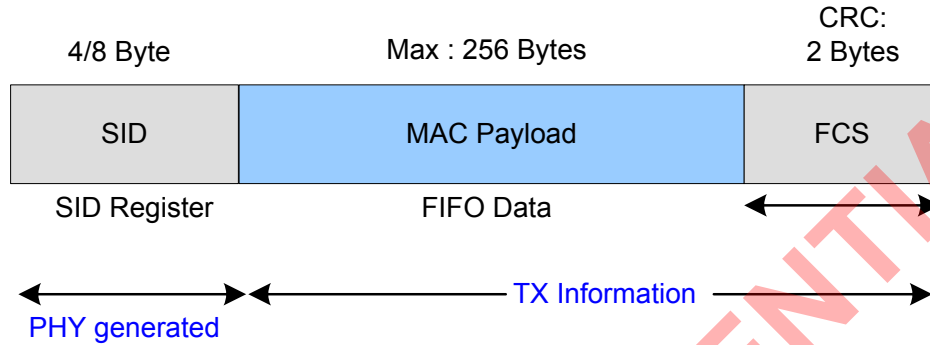
10.4 Frame Structure

As below TRX format, the A8125M0 contains:

- Serial Packet ID (SID), the length is 4/8 bytes.

- The physical FIFO depth is 64 bytes and it can supports logical FIFO extension up to 256 bytes.
- If CRC is enabled (CRCS=1), 2-bytes of CRC value is transmitted automatically after payload. In the same way, RX circuitry will check CRC value and show the result to CRC Flag.

TX format



RX format

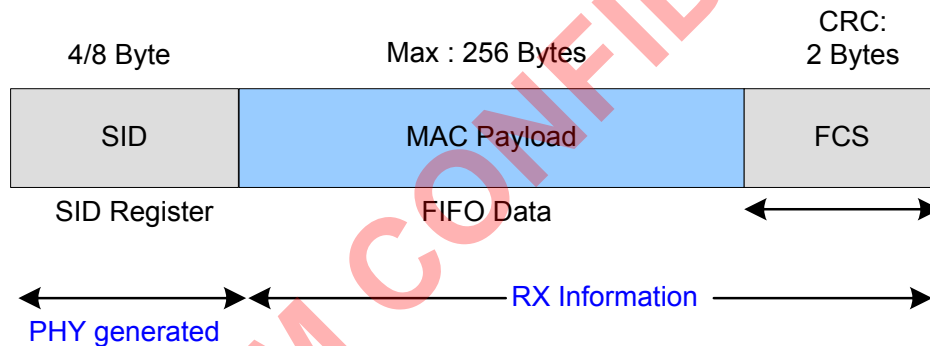


Figure 10.1 TRX format

10.5 Transceiver Frequency

A8125M0 is a half-duplex transceiver with embedded PA and LNA. For TX or RX frequency setting, user just needs to set up LO frequency for two ways radio transmission.

A8125M0's main PLL features are:

- Fractional-N to generate RX/TX frequencies for all ISM 2.4 GHz channels
- Auto calibration loops for stable operation within the operating range
- Fast PLL settling to support frequency hopping

During receive operation, the frequency synthesizer works as a local oscillator. During transmit operation, the voltage-controlled oscillator (VCO) is directly modulated to generate the RF transmit signal. The frequency synthesizer is implemented as a fractional-N PLL.

A8125M0's LO frequency $F_{LO} = F_{LO_BASE} + F_{OFFSET}$. Where

$$F_{LO_BASE} = F_{PFD} * (BIP[8:0] + \frac{BFP[15:0]}{2^{16}}) * 2 = \frac{F_{XTAL}}{RRC[1:0] + 1} * (BIP[8:0] + \frac{BFP[15:0]}{2^{16}}) * 2$$

$F_{OFFSET} = CHN * F_{CHSP}$, and

$$F_{CHSP} = F_{PFD} \times \frac{CHR}{2^{16}} \times 2$$

Therefore, A8125M0 is very easy to implement frequency hopping by **ONE register setting, (CHN)**. In general, user can plan the wanted channels by a CHN Look-Up-Table between master and slaves for two-way frequency hopping.

10.6 State machine

A8125M0 supports 6 key operation states. That is,

- (1) Sleep MODE
- (2) Reserved MODE
- (3) Standby MODE
- (4) PLL MODE
- (5) RX MODE
- (6) TX MODE

After power on reset or software reset, user has to do calibration process because all control registers are in initial values. The calibration process of A8125M0 is very easy, user only needs to issue Strobe commands and enable calibration registers. After calibration, A8125M0 is ready to do TX and RX operation. User can start wireless transmission.

Strobe Command								Description
b7	b6	b5	b4	b3	b2	b1	b0	
1	0	0	0	x ^{*1}	x	x	x	Sleep MODE
1	0	0	1	x	x	x	x	Reserved MODE
1	0	1	0	x	x	x	x	Standby MODE
1	0	1	1	x	x	x	x	PLL MODE
1	1	0	0	x	x	x	x	RX MODE
1	1	0	1	x	x	x	x	TX MODE

MODE	RF Register retention	RF Regulator	Xtal Osc.	VCO	PLL	RX	TX	Strobe Command
Sleep	Yes	ON	ON ^{*2}	OFF	OFF	OFF	OFF	(1000-xxxx)b
Reserved	Yes	ON	ON	OFF	OFF	OFF	OFF	(1001-xxxx)b
Standby	Yes	ON	ON	OFF	OFF	OFF	OFF	(1010-xxxx)b
PLL	Yes	ON	ON	ON	ON	OFF	OFF	(1011-xxxx)b
RX	Yes	ON	ON	ON	ON	ON	OFF	(1100-xxxx)b
TX	Yes	ON	ON	ON	ON	OFF	ON	(1101-xxxx)b

Note 1: x means "don't care".

Note 2: MCU in non-stop mode. If MCU also in stop mode, it will enter PM mode and crystal oscillator is off.

Table 10.1 Operation MODE and strobe command.

10.7 FIFO mode

This MODE is suitable for the requirements of general purpose applications and can be chosen by setting FMS = 1. After calibration, user can issue Strobe command to enter standby MODE where write TX FIFO or read RX FIFO. From standby MODE to packet data transmission, only one Strobe command is needed. Once transmission is done, A8125M0 is auto back to standby MODE.

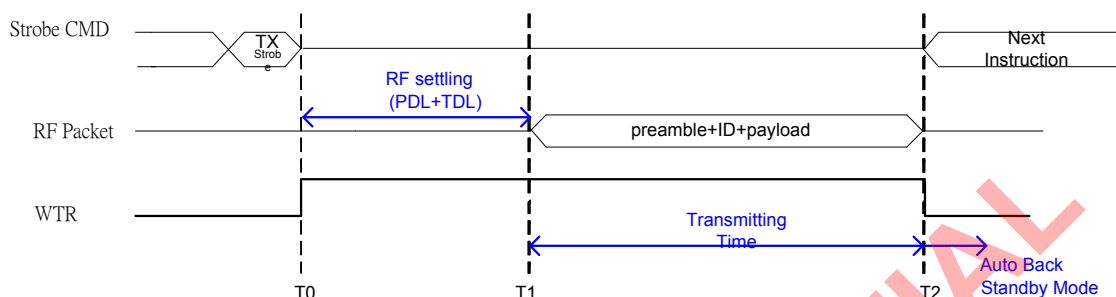


Figure 10.2 TX timing of FIFO MODE.

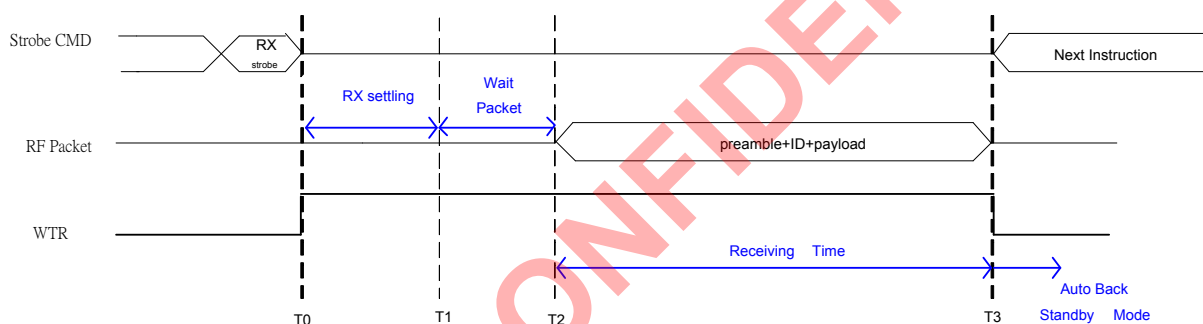


Figure 10.3 RX timing of FIFO MODE.

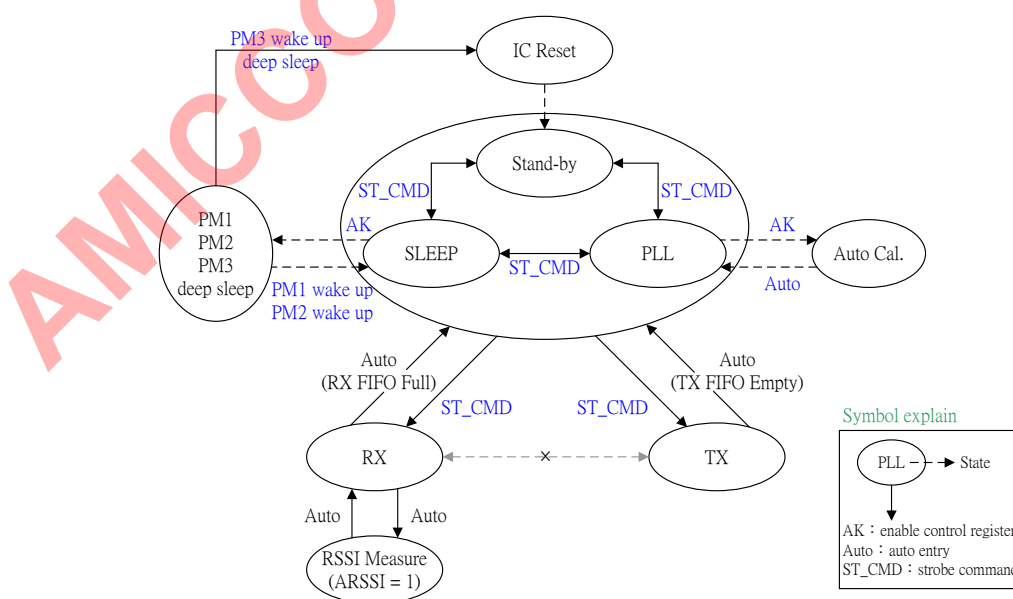


Figure 10.4 State diagram of FIFO Mode.

10.8 Calibration

A8125M0 needs calibration process after reset. Below are seven calibration items inside the device.

1. VCO Current Calibration.
2. VCO Bank Calibration.
3. VCO Deviation Calibration.
4. IF Filter Bank Calibration.
5. RC Oscillator (WOR) Calibration.
6. RSSI Calibration
7. ADC Calibration

10.8.1 Calibration Procedure

The purpose to execute the above calibration items is to deal with Foundry process deviation. After calibrations, A8125M0 will be set to the best working conditions without concerning Foundry process deviation to impact A8125M0's RF performance.

In general, user can use A8125M0's auto calibration function by just enabling calibration items and checking its calibration flag. For detailed calibration procedures, please refer to A8125M0 reference code of InitRF() subroutine.

Initialize A8125M0 by calling the subroutine of InitRF().

Note:

1. VCO calibration should be executed in PLL mode.(Others in STBY mode)
2. After IF calibration, RF should be return SLEEP mode once for reset main clock phase.

11. SoC Architectural Overview

A8125M0 build-in the ARM® Cortex™-M0 that implements the ARMv6-M Thumb® instruction set, including Thumb-2 technology. This provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density. The Cortex-M0 processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance.

A8125M0 integrates many features such as two 32bit counters/timers, 16/32bits dual-timer, watchdog timer, RTC, UART, SPI interface, I²C interface, 8 channels PWM, 8 channels 12bits ADC and battery detector.

A8125M0 includes SWD debug circuitry that provides full time, real-time, in-circuit debugging.

11.1 ARM® Cortex™-M0

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor which has an AMBA AHB-Lite interface and includes an NVIC component.

The processor can execute Thumb code and is compatible with other Cortex™-M0 profile processors. The profile supports two modes - Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset and can be entered as a result of an exception return. The following figure shows the functional controller of the processor.

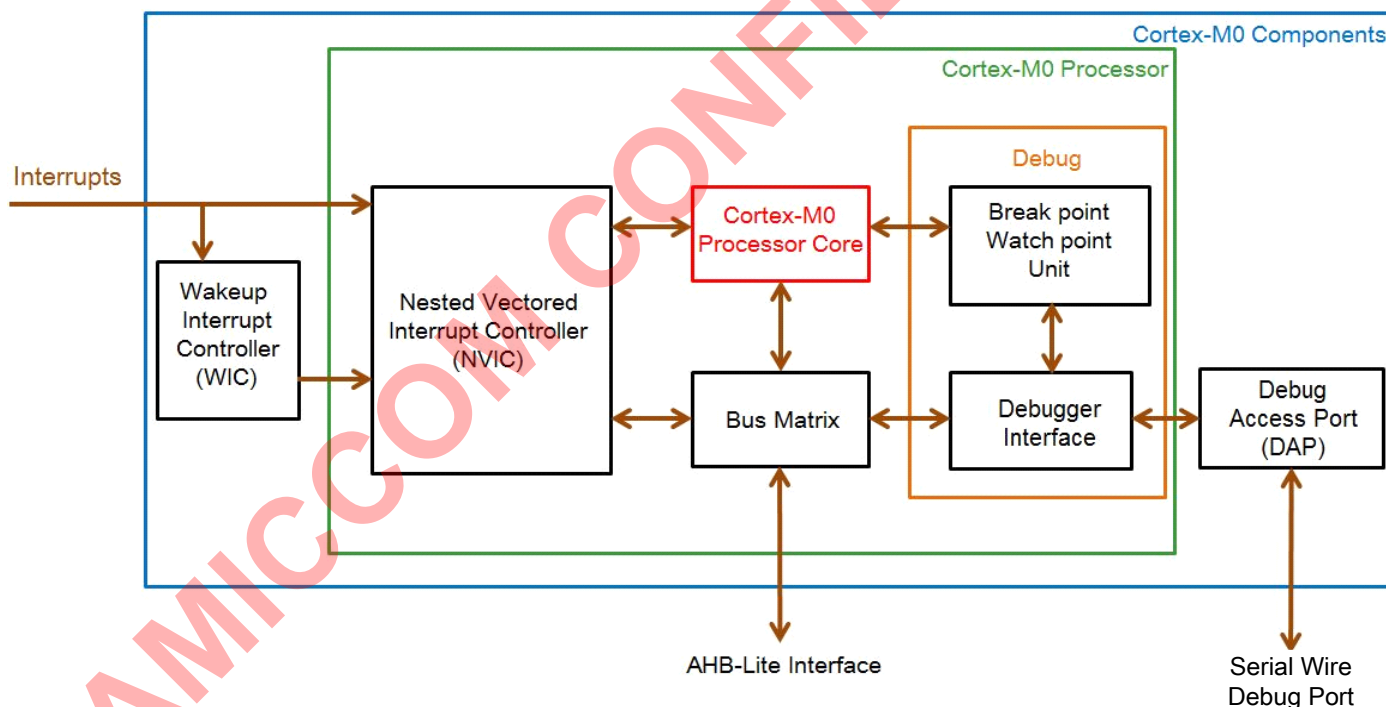


Figure 11.1 Core-M0 block diagram

11.1.1 Feature

- ◆ A low gate count processor
 - ARMv6-M Thumb® instruction set
 - Thumb-2 technology
 - ARMv6-M compliant 24-bit SysTick timer
 - A 32-bit hardware multiplier

- System interface supported with little-endian data accesses
- Ability to have deterministic, fixed-latency, interrupt handling
- Load/store-multiples and multicycle-multiples that can be abandoned and restarted to facilitate rapid interrupt handling
- ◆ NVIC
 - Up to 32 external interrupt inputs, each with four levels of priority
 - Dedicated Non-Maskable Interrupt (NMI) input
 - Supports for both level-sensitive and pulse-sensitive interrupt lines
- ◆ Debug support
 - Four hardware breakpoints
 - Two watch points
 - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
 - Single step and vector catch capabilities
 - Full access to core registers when the processor is halted
- ◆ Bus interfaces
 - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
 - Single 32-bit slave port that supports the DAP (Debug Access Port)

11.2 Memory Organization

The memory organization is shown as figure 11.2

0xFFFF_FFFF	Reserved
0xE010_0000	Private Peripheral Bus
0xE000_0000	Reserved
0x5000_0000	AHB Peripherals
0x4008_0000	Reserved
0x4000_0000	APB Peripherals
	Reserved
0x2000_0000	RAM
	Reserved
0x1000_1000	UICR
	Reserved
0x1000_0000	FICR
	Reserved
0x0000_0000	Code

Figure 11.2 Memory Organization

11.3 Nested Vectored Interrupt Controller (NVIC)

The Cortex™-M0 CPU provides an interrupt controller as an integral part of the exception mode, named as “Nested Vectored Interrupt Controller (NVIC)”, which is closely coupled to the processor core and provides following features.

11.3.1 Feature

- Flexible interrupt management

In the Cortex-M0 processor, each external interrupt can be enabled or disabled and can have its pending status set or clear by software. It can also accept exception requests at signal level (interrupt request from a peripheral remain asserted until the interrupt service routine clears the interrupt request), as well as an exception request pulse (minimum 1 clock cycle). This allows the interrupt controller to be used with any interrupt source.

- Nested interrupt support

In the Cortex-M0 processor, each exception has a priority level. The priority level can be fixed or programmable. When an exception occurs, such as an external interrupt, the NVIC will compare the priority of this exception to the current level. If the new exception has a higher priority, the current running task will be suspended. Some of the registers will be stored on to the stack memory, and the processor will start executing the exception handler of the new exception. This process is called “preemption.” When the higher priority exception handler is complete, it is terminated with an exception return operation and

the processor automatically restores the registers from the stack and resumes the task that was running previously. This mechanism allows nesting of exception services without any software overhead.

- Vectored exception entry

The Cortex-M0 automatically locates the starting point of the exception handler from a vector table in the memory. As a result, the delay from the start of the exception to the execution of the exception handlers is reduced.

- Interrupt masking

The NVIC in the Cortex-M0 processor provides an interrupt masking feature via the PRIMASK special register. This can disable all exceptions except hard fault and NMI. This masking is useful for operations that should not be interrupted such as time critical control tasks or real-time multimedia codecs.

11.3.2 Exception Types and Interrupt Map

Each exception source in the Cortex-M0 processor has a unique exception number. The exception number for NMI is 2, and the exception numbers for the on-chip peripherals and external interrupt sources are from 16 to 47. The other exception numbers, from 1 to 15, are for system exceptions generated inside the processor, although some of the exception numbers in this range are not used. Each exception type also has an associated priority. The priority levels of some exceptions are fixed and some are programmable. Table 11.1 shows the exception types, exception numbers, and priority levels.

Exception Number	Exception Type	Priority	Interrupt Description
1	Reset	-3(Highest)	Reset
2	NMI	-2	Non Maskable interrupt
3	Hard fault	-1	Fault handling exception
4-10	Reserved	--	--
11	SVC	Programmable	Supervisor call via SVC instruction
12-13	Reserved	--	--
14	PendSV	Programmable	Pendable request for system service
15	SysTick	Programmable	System tick timer
16-47	IRQ0~IRQ31	Programmable	IRQ

Table 11.1 Exception Types

Exception Number	Interrupt Number Bit	Interrupt Name	Interrupt Description
16	0	--	-
17	1	UART0_INT	UART0 Tx/Rx/Overrun interrupt
18	2	--	--
19	3	RADIO_INT	RADIO interrupt
20	4	--	--
21	5	UART2_INT	UART2 Tx/Rx/Overrun interrupt
22	6	GPIO0_INT	GPIO0 interrupt
23	7	--	--
24	8	TIMER0_INT	Timer0 interrupt
25	9	TIMER1_INT	Timer1 interrupt
26	10	Dual_Timer_INT	Dual Timer interrupt
27	11	--	--
28	12	--	--
29	13	UART1_INT	UART1 Tx/Rx/Overrun interrupt
30	14	--	--
31	15	NFC_INT	NFC interrupt
32	16	SPI0_INT	SPI0 interrupt
33	17	I ² C_INT	I ² CM/I ² CS interrupt
34	18	--	--
35	19	SPI1_INT	SPI1 interrupt
36	20	--	--
37	21	ADC_INT	12bits-ADC interrupt
38	22	RCADC_INT	24bits-RCADC interrupt
39	23	--	--
40	24	--	--
41	25	--	--
42	26	--	--
43	27	--	--
44	28	--	--
45	29	--	--
46	30	--	--
47	31	--	--

Table 11.2 Interrupt Map Vector Table

11.4 Reset source

Reset circuitry allows A8125M0 to be easily placed in a predefined default condition. LVD, Reset, POR, NVIC reset, and Watchdog signal will reset A8125M0 when they happen.

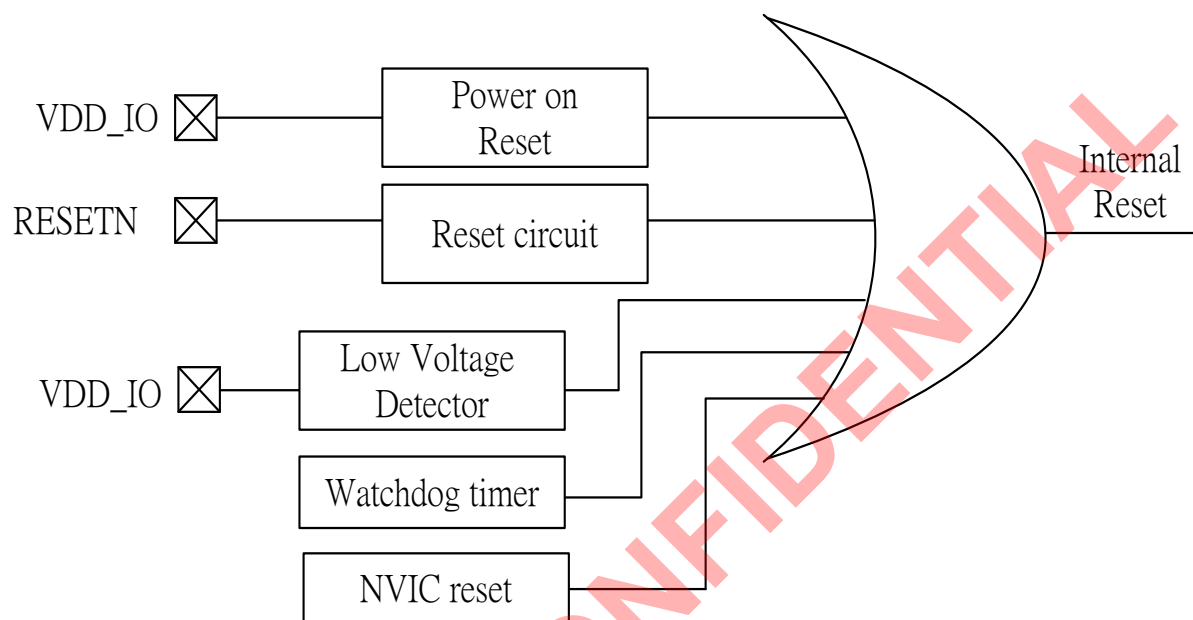


Figure 11.3 Reset source

11.5 Clock Source

A8125M0 has three clock source like crystal oscillator (XI, XO), RTC crystal (P0.22, P0.23/ RTC_I, RTC_O) and internal RC oscillator. In the MCU part (digital peripherals), user chooses the suitable clock source by power consumptions and performance. In the RF part, the clock source only comes from XTAL.

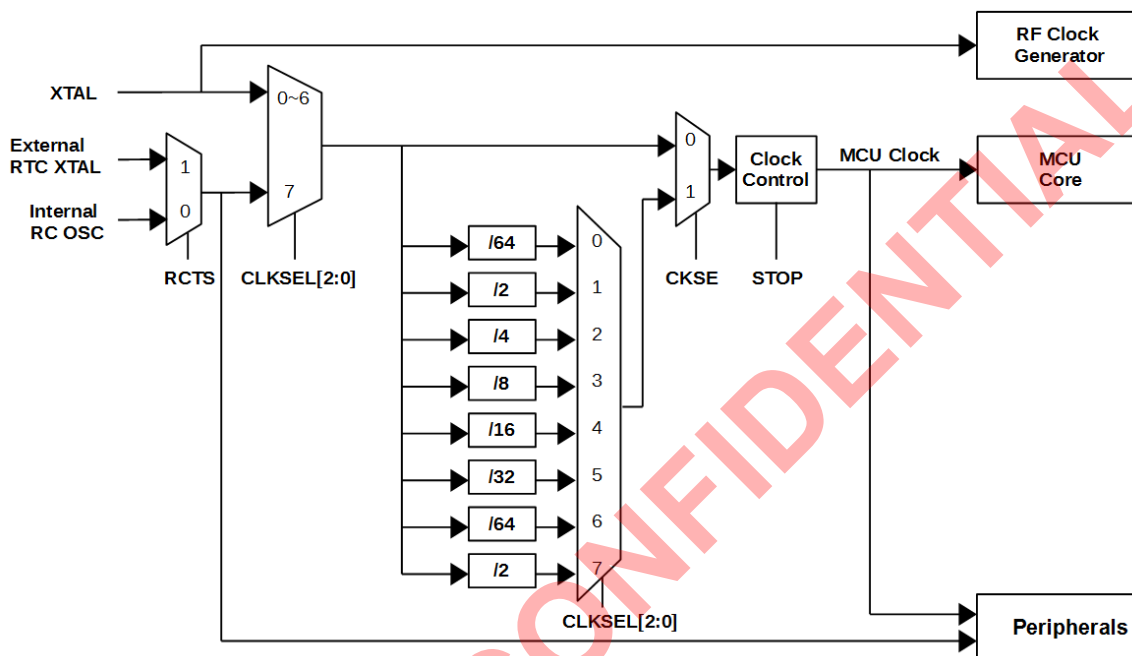


Figure 11.4 Whole chip clock

11.6 System Timer (SysTick)

The SysTick timer is a 24-bit down counter. It reloads automatically after reaching zero, and the reload value is programmable. When reaching zero, the timer can generate a SysTick exception (exception number 15). For the CortexTM-M0 processor, a simple timer called the SysTick is included to generate this regular interrupt request.

11.6.1 SysTick Control and Status Register (Address:0xE000E010)

R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W	--							
R	--							
Reset	0	0	0	0	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	--							COUNTFLAG
R	--							COUNTFLAG
Reset	0	0	0	0	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	--							
R	--							
Reset	0	0	0	0	0	0	0	0
R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--					CLKSOURCE	TICKINT	ENABLE
R	--					CLKSOURCE	TICKINT	ENABLE
Reset	0	0	0	0	0	0	0	0

COUNTFLAG: Returns 1 if timer counted to 0 since the last read of this register.

CLKSOURCE : Selects the SysTick timer clock source

0 = external reference clock
 1 = processor clock.
 CLKSOURCE needs to be set 1 when uses SysTick.

TICKINT: Enables SysTick exception request
 0 = counting down to zero does not assert the SysTick exception request
 1 = counting down to zero to asserts the SysTick exception request.

ENABLE: Enables the counter
 0 = counter disabled
 1 = counter enabled.

11.6.2 SysTick Reload Value Register (Address:0xE000E014)

R/W	Bit 31	-----	Bit 24	Bit 23	-----	Bit 0
W	--				--	
R	--				RELOAD[23:0]	
Reset	0x0				0x000	

RELOAD[23:0]: Value to load into the SysTick when the counter is enabled and when it reaches 0.

11.6.3 SysTick Current Value Register (Address:0xE000E018)

R/W	Bit 31	-----	Bit 24	Bit 23	-----	Bit 0
W	--				--	
R	--				CURRENT[23:0]	
Reset	0x0				0x000	

CURRENT[23:0]: Reads return the current value of the SysTick counter.

11.7 Slow Clock Source

A8125M0 support two slow clock sources: internal RC oscillator and extern RTC crystal. User can set RCTS=0 or 1 to select internal RC-OSC or external RTC-XTAL. Slow clock source is the clock source for slow peripherals to keep working when MCU enter PM (power management) mode. For example: Sleep Timer, Real Timer Counter

11.7.1 Turn on External RTC XTAL

User can follow the step as blow to turn on external RTC XTAL:

1. PULLHIGHSET (0x40010008) = (1<<22) | (1<<23)
2. POALTFUNCSET (0x40010018) = (1<<22) | (1<<23)
3. RCCTRL1 (0x50000040) = 0x00000000
4. RCCTRL1 (0x50000040) = 0x0000008C (Set RCOT=1, RCTS=1, ROE=1)
5. Delay sometime for External RTC XTAL stable (about 100ms, depend on RTC XTAL)

11.7.2 Turn on Internal RC OSC

User can follow the step as blow to turn on internal RC OSC:

1. RCCTRL1 (0x50000040) = 0x00
2. RCCTRL2 (0x50000040) = 0x00000004 (Set ROE=1)
3. RCTARGET (0x50000044) = 977 (for 32.768KHz) or 1000 (for 32KHz)
4. RCCTRL1 (0x50000040) = 0x00000105 (Set ENCAL=1, ROE=1, RCKS0=1)
5. Check RCCTRL1 until ENCAL auto clear to 0 (about 10ms)

IRC clock formula:

$$\frac{IRC\ clock}{2} = \frac{16MHz}{TGNUM[13:0]}$$

12. I/O Ports

12.1 FEATURE

- Tri-state GPIO (input, output high, output low)
- Support Pull-up resistor
- Support Wakeup pin
- Support 4 types GPIO Interrupt
- Support High Driving Current Output
- Support 24GPIO and Key wake-up

12.2 BLOCK DIAGRAM

Each GPIO has the same structure as below:

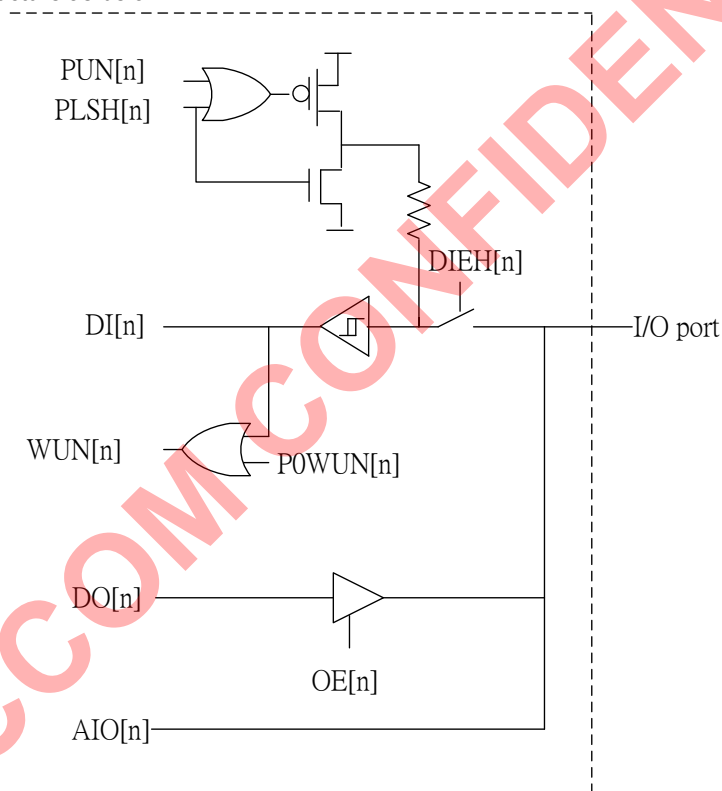


Figure 12.1 I/O Block Diagram

12.3 REGISTER

12.3.1 Register List

Address	Name	DESCRIPTION
0x40010000	P0DATA	Port 0 Data Register
0x40010004	P0DATAOUT	Port 0 Data Out Register
0x40010008	P0PUN	Port 0 Pull Up Not Register
0x4001000C	P0WUN	Port 0 Wakeup Enable Not Register
0x40010010	P0OUTENABLESET	Port 0 Output Enable Set Register
0x40010014	P0OUTENABLECLR	Port 0 Output Enable Clear Register
0x40010018	P0ALTFUNCSET	Port 0 Alternative Function Set Register
0x4001001C	P0ALTFUNCCLR	Port 0 Alternative Function Clear Register
0x40010020	P0INTENSET	Port 0 Interrupt Enable Set Register

0x40010024	POINTENCLR	Port 0 Interrupt Enable Clear Register
0x40010028	POINTTYPESET	Port 0 Interrupt Type Set Register
0x4001002C	POINTTYPECLR	Port 0 Interrupt Type Clear Register
0x40010030	POINTPOLSET	Port 0 Interrupt Polarity Set Register
0x40010034	POINTPOLCLR	Port 0 Interrupt Polarity Clear Register
0x40010038	POINTSTATUS	Port 0 Interrupt Request Status Register

Table 12.1 GPIO0 Register list

12.3.2 Register Description

- A8125M0 support P0.0 ~P0.23 only.

P0DATA (Port 0 Data Register)

Address: 0x40010000

R/W	Bit 31	-----	Bit 0
W		P0DATAOUT [31:0]	
R		P0DATA [31:0]	
Reset		0x00000000	

P0DATAOUT[31:0]: Port 0 data out (output data, DO)

P0DATA[31:0]: Port 0 data (input data, DI)

P0DATAOUT (Port 0 Data Out Register)

Address: 0x40010004

R/W	Bit 31	-----	Bit 0
W		P0DATAOUT [31:0]	
R		P0DATAOUT [31:0]	
Reset		0x00000000	

P0DATAOUT[31:0]: Port 0 data out (output data, DO)

P0PUN (Port 0 Pull Up Not Register)

Address: 0x40010008

R/W	Bit 31	-----	Bit 0
W		P0PUN [31:0]	
R		P0PUN [31:0]	
Reset		0x00000000	

P0PUN[31:0]: Port 0 Pull Up Not

[0]: Pull up resistor enable (input setting usually).

[1]: Pull up resistor disable (output setting usually)

P0WUN (Port 0 Wakeup Enable Not Register)

Address: 0x4001000C

R/W	Bit 31	-----	Bit 0
W		P0WUN [31:0]	
R		P0WUN [31:0]	
Reset		0xFFFFFFFF	

P0WUN[31:0]: Port 0 Wake Up Enable Not

[0]: IO pin wakeup enable

[1]: IO pin wakeup disable

P0OUTENABLESET (Port 0 Output Enable Set Register)

Address: 0x40010010

R/W	Bit 31	-----	Bit 0
W		P0OUTENABLESET [31:0]	
R		P0OUTENABLE [31:0]	
Reset		0x00000000	

P0OUTENABLESET [31:0]: Port 0 Output Enable Set

[0]: No effect
[1]: Output enable set. (Set IO pin to output)

P0OUTENABLE[31:0]: Port 0 Output Enable

[0]: IO pin is input
[1]: IO pin is output.

P0OUTENABLECLR (Port 0 Output Enable Clear Register)

Address: 0x40010014

R/W	Bit 31	-----	Bit 0
W	P0OUTENABLECLR [31:0]		
R	P0OUTENABLE [31:0]		
Reset	0x00000000		

P0OUTENABLECLR [31:0]: Port 0 Output Enable Clear

[0]: No effect
[1]: Output enable clean (set IO pin to input).

P0OUTENABLE[31:0]: Port 0 Output Enable

[0]: IO pin is input
[1]: IO pin is output.

P0ALTFUNCSET (Port 0 Alternative Function Set Register)

Address: 0x40010018

R/W	Bit 31	-----	Bit 0
W	P0ALTFUNCSET [31:0]		
R	P0ALTFUNC [31:0]		
Reset	0x00000000		

P0ALTFUNCSET [31:0]: Alternative function set

[0]: No effect
[1]: Alternative function set (alternative function enable).

P0ALTFUNC[31:0]: Alternative function status

[0]: Alternative function disable (GPIO).
[1]: Alternative function enable (Multi-function IO)

P0ALTFUNCCLR (Port 0 Alternative Function Clear Register)

Address: 0x4001001C

R/W	Bit 31	-----	Bit 0
W	P0ALTFUNCCLR [31:0]		
R	P0ALTFUNC [31:0]		
Reset	0x00000000		

P0ALTFUNCCLR [31:0]: Alternative function clear

[0]: No effect
[1]: Alternative function clean (alternative function disable)..

P0ALTFUNC[31:0]: Alternative function status

[0]: Alternative function disable (GPIO)
[1]: Alternative function enable (Multi-function IO)

P0INTENSET (Port 0 Interrupt Enable Set Register)

Address: 0x40010020

R/W	Bit 31	-----	Bit 0
W	P0INTENSET [31:0]		
R	P0INTEN [31:0]		
Reset	0x00000000		

P0INTENSET[31:0]: Port 0 interrupt enable set

[0]: No effect

[1]: Interrupt enable set (interrupt enable)

POINTEN[31:0]: Port 0 interrupt enable status

[0]: Interrupt disable

[1]: Interrupt enable

POINTENCLR (Port 0 Interrupt Enable Clear Register)

Address: 0x40010024

R/W	Bit 31	-----	Bit 0
W		POINTENCLR [31:0]	
R		POINTEN [31:0]	
Reset		0x00000000	

POINTENCLR[31:0]: Port 0 interrupt enable clear

[0]: No effect

[1]: Interrupt enable clear (interrupt disable)

POINTEN[31:0]: Port 0 interrupt enable status

[0]: Interrupt disable

[1]: Interrupt enable

POINTTYPESET (Port 0 Interrupt Type Set Register)

Address: 0x40010028

R/W	Bit 31	-----	Bit 0
W		POINTTYPESET [31:0]	
R		POINTTYPE [31:0]	
Reset		0x00000000	

POINTTYPESET[31:0]: Port 0 interrupt type set

[0]: No effect

[1]: Interrupt type set (interrupt by edge)

POINTTYPE[31:0]: Port 0 interrupt type status

[0]: Interrupt by level

[1]: Interrupt by edge

POINTTYPECLR (Port 0 Interrupt Type Clear Register)

Address: 0x4001002C

R/W	Bit 31	-----	Bit 0
W		POINTTYPECLR [31:0]	
R		POINTTYPE [31:0]	
Reset		0x00000000	

POINTTYPECLR[31:0]: Port 0 interrupt type clear

[0]: No effect

[1]: Interrupt type clear (interrupt by level).

POINTTYPE[31:0]: Port 0 interrupt type status

[0]: Interrupt by level

[1]: Interrupt by edge

POINTPOLSET (Port 0 Interrupt Polarity Set Register)

Address: 0x40010030

R/W	Bit 31	-----	Bit 0
W		POINTPOLSET [31:0]	
R		POINTPOL [31:0]	
Reset		0x00000000	

POINTPOLSET[31:0]: Port 0 interrupt level set

[0]: No effect

[1]: Polarity-level set (high level or rising edge)

POINTPOL[31:0]: Port 0 interrupt level status

[0]: Low level or falling edge

[1]: High level or rising edge

POINTPOLCLR (Port 0 Interrupt Polarity Clear Register)

Address: 0x40010034

R/W	Bit 31	-----	Bit 0
W		POINTPOLCLR [31:0]	
R		POINTPOL [31:0]	
Reset		0x00000000	

POINTPOLCLR[31:0]: Port 0 interrupt level clear

[0]: No effect

[1]: Polarity-level clean (low level or falling edge)

POINTPOL[31:0]: Port 0 interrupt level status

[0]: Low level or falling edge

[1]: High level or rising edge

POINTSTATUSCLR (Port 0 Interrupt Request Status Register)

Address: 0x40010038

R/W	Bit 31	-----	Bit 0
W		POINTSTATUSCLR [31:0]	
R		POINTSTATUS [31:0]	
Reset		0x00000000	

POINTSTATUSCLR[31:0]: Port 0 interrupt request clear

[0]: No effect

[1]: Clear interrupt request status

POINTSTATUS[31:0]: Port 0 interrupt request status

[0]: No interrupt request

[1]: An interrupt request has occurred

12.4 FUNCTION DESCRIPTION

12.4.1 Output Enable (OE)

Each port has 32pins digital I/O Pins and each pin of port can be defined as general-purpose I/O (GPIO) or peripheral I/O signals connected to the timers, UART, I²C and SPI functions. Thus, each pin can also be used to wake up from PM mode.

User can select each pin function by setting register. Each port has itself port register like P0DATA (0x40010000). When reading, the logic levels of the Port's input pins are returned. As shown the below Table 12.2 and Table 12.3, each port has three registers to setting Pull-Up Not (PUN), Output-Enable (OE) and Wakeup enable Not (WUN). As shown the below block diagram, Figure 12.1 I/O Block . Unused I/O pins should have a defined level and not be left floating. One way to do this is to leave the pin unconnected and configure the pin as a general-purpose I/O input with pull-up resistor.

According the Table 12.2, all pins can be configured as Output, Input or Input with the pull-up resistor (around 100 Kohm). Please refer the Table 12.2 truth table to know every function setting. When OE=1, this pin is configured as Output. Otherwise OE=0, this pin is configured as Input. User can set PUN=1 or 0 depending on application. When OE=0, PUN=0 is recommended for saving power.

OE[n]	PUN[n]	I/O port status
0	0	input with pull high
0	1	input without pull high
1	1	output

Table 12.2 I/O Port setting

P0WUN[n]	Wake up (WUN)
0	Enable*
1	Disable

* The I/O port must set to input(i.e. OE = 0).

Table 12.3 WUN setting

12.4.2 Wake up function(WUN)

MCU can wake up from PM1, PM2, PM3 and deep sleep by WUN function. WUN supports four types. The setting of edgts shows as table 12.4. PM1, PM2 and PM3 can wake up by all port pin. Deep sleep only wake up by P0.14 ~ P0.17. PM3 and deep sleep will reset peripherals after wake up.

User can use P0 port as key input. It is a helpful use to design a remote controller and low power consumption with power saving mode setting. **Note: This function is used by PM mode only. Furthermore, it don't occurred exception.**

EDGTS[1:0]	WUN by
00	Both positive and negative edge
01	PLSH= 0: Negative edge PLSH= 1: Positive edge
10	PLSH= 0: Positive edge PLSH= 1: Negative edge
11	Level

Table 12.4 WUN_edgts setting table

12.4.3 GPIO0 interrupt (GPIO0_INT)

The NVIC IRQn of GPIO0_INT is 6. Please refer Table 11.2 Interrupt Map Vector Table. This interrupt can't wakeup MCU. GPIO0_INT supports 4 types IO interrupt. **It needs work on normal mode.** The setting of GPIO0_INT shows as Table 12.5

P0INTTYPE	P0INTPOL	Interrupt by
0	0	Low level
0	1	High Level
1	0	Falling Edge
1	1	Rising Edge

Table 12.5 Port 0 interrupt setting table

12.4.4 IO mode select (DSSPILH)

All port pin can select pull-high and pull-low state. In input state, DIEHx need to select input. On the contrary, set up tri-state. If user wants to set up IO DATA value as high, PLSHx need to select pull-high. On the contrary, select pull-low.

Example:

HW32_REG(0x50000024) = 0x00001F1F;

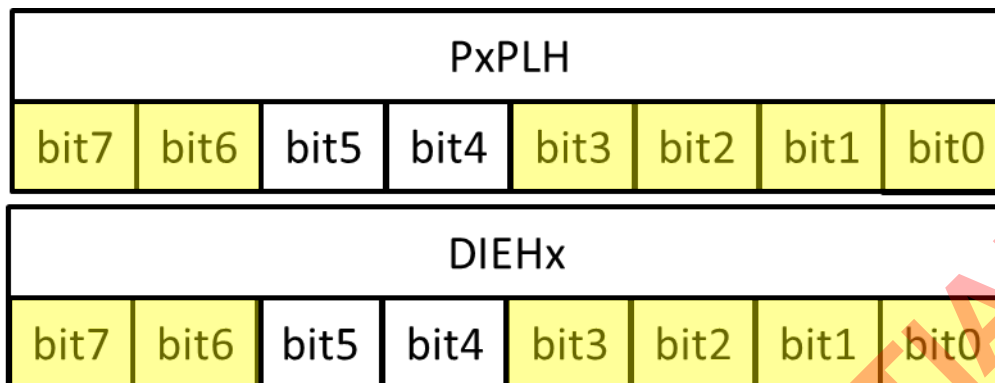
P0.4 ~ P0.0 set up Px input enable & pull low , P0.7 ~ P0.5 set up tri-state & pull high

PxPLH							
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0

DIEHx							
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0

HW32_REG(0x50000024) = 0x00001FCF;

P0.7 ~ P0.6 & P0.4 ~ P0.0 set up Px input enable & pull low



WBUS[7:0] control PxPLH and DIEHx, respectively. PxLH and PxPLH are latch value, that set up high will auto latch value.

12.4.5 Debug Interface and Flash Mask

There are four IO pins need to notice: P0_06, P0_07, P0_13 and P0_12

- P0_06, P0_07 will be set to SWDIO and SWCLK when P0_12 = 0 at reset.
- Flash will be mask (read out 0xFFFFFFFF) when P0_12=0 and P0_13=0 at reset.

GPIO pins	At Reset				After Rest	
	P0_12	P0_06	P0_07	P0_13	IO Pins	Flash
P0_12	1	X	X	X	P0_12	Flash not mask
P0_06					P0_06	
P0_07					P0_07	
P0_13					P0_13	
P0_12	0	X	X	1	P0_12	Flash not mask
P0_06					SWDIO	
P0_07					SWCLK	
P0_13					P0_13	
P0_12	0	X	X	0	P0_12	Flash MASKED
P0_06					SWDIO	
P0_07					SWCLK	
P0_13					P0_13	

Table 12.6 The pins for debug interface and flash mask

Flash mask is a special measure when the MCU can't download code because of a program execution. User can use Flash Mask to mask flash ROM and erase flash ROM. Please pay attention to the use of restrictions when planning the circuit.

13. Timer

13.1 FEATURE

- Programmable 32-bits Timer
- Interrupt generator
- Support input-edge count or time-capture

13.2 PINS DESCRIPTION

PIN	GPIO	TYPE	DESCRIPTION
TIMER0EIN	P0_08	INPUT	EXTIN (external input) for Timer0
TIMER1EIN	P0_09	INPUT	EXTIN (external input) for Timer1

13.3 BLOCK DIAGRAM

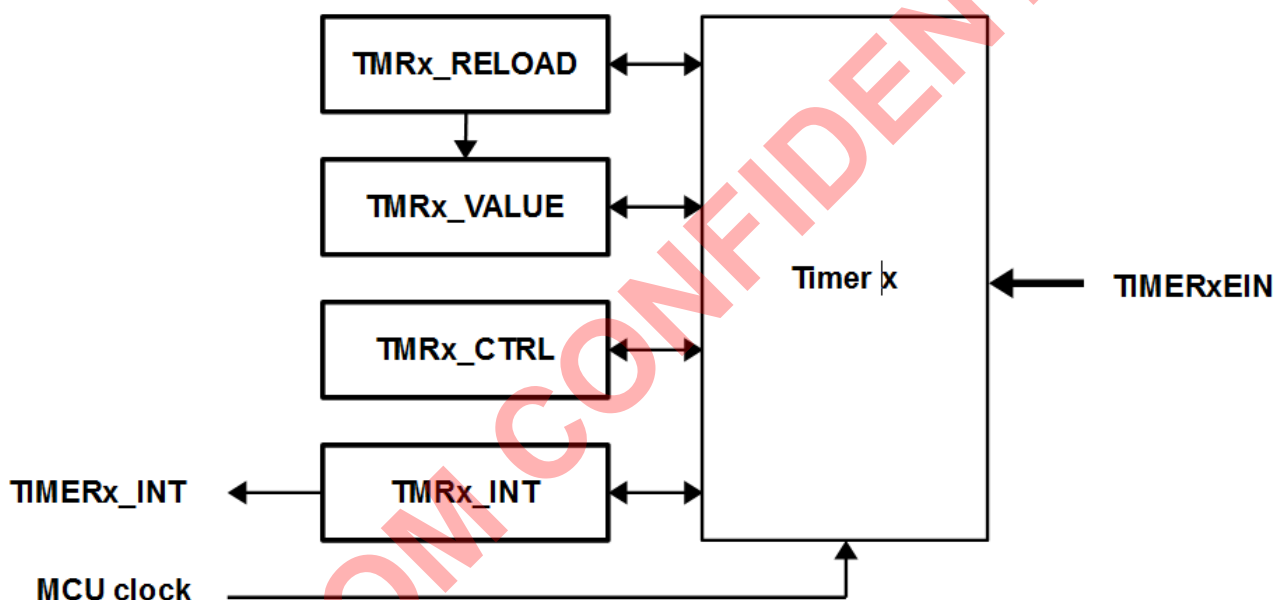


Figure 13.1 32-Bit Timer/Counter block diagram

13.4 REGISTER

13.4.1 Base Address List

Base Address	DESCRIPTION
0x40000000	TIMER0 Base address
0x40001000	TIMER1 Base address

Table 13.1 Base address list

13.4.2 Register List

offset	Name	DESCRIPTION
0x000	TMRx_CTRL	Timer x Control Register
0x004	TMRx_VALUE	Timer x Current Value Register
0x008	TMRx_RELOAD	Timer x Reload Register
0x00C	TMRx_INT	Timer x Interrupt Status Register

Table 13.2 Register list

13.4.3 Register Description

TMRx_CTRL (Timer x Control Register)

Offset: 0x000

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--				CTRL [3:0]			
R								
Reset	0	0	0	0	0	0	0	0

CTRL[0]: Enable decrement control

[0]: Disable (Timer stop decrement)

[1]: Enable (Timer start decrement)

CTRL[1] : Select external input as enable

[0]: Disable

[1]: Enable (Timer stop when EXTIN=0)

CTRL[2] : Select external input as clock

[0]: Disable

[1]: Enable (Timer decrement when EXTIN rising edge)

CTRL[3] : Timer interrupt enable.

[0]: Disable

[1]: Enable

TMRx_VALUE (Timer x Current Value Register)

Offset: 0x004

R/W	Bit31	-----	Bit 0
W	VALUE [31:0]		
R			
Reset	0x00000000		

VALUE[31:0]: Current counter value.

TMRx_RELOAD (Timer x Reload Register)

Offset: 0x008

R/W	Bit31	-----	Bit 0
W	RELOAD [31:0]		
R			
Reset	0x00000000		

RELOAD [31:0]: Reload value. VALUE[31:0] will be wrote when write RELOAD [31:0] immediately.

TMRx_INT (Timer x Interrupt Status Register)

Offset: 0x00C

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--							INTCLEAR
R								INTSTATUS
Reset	0	0	0	0	0	0	0	0

INTCLEAR:

[0]: No effect

[1]: Clear INTSTATUS

INTSTATUS: interrupt status (TIMERINT status)

[0]: Interrupt not occur

[1]: Interrupt occur

13.5 FUNCTION DESCRIPTION

13.5.1 VALUE and RELOAD

When any value write to RELOAD[31:0], the VALUE[31:0] will be wrote to the same value immediately. When timer CTRL[0]=1, the VALUE[31:0] start count-down with MCU clock or EXTIN rising edge. When VALUE[31:0] count-down to 0, the VALUE[3:0] will be wrote with RELOAD[31:0] in next clock or rising edge. Please refer Figure 13.2.

13.5.2 Input-edge Counter

When CTRL[2]=1, Timer is in input-edge count mode. The value of Timer will count down when EXTIN rising edge. The interrupt will occur when VALUE[31:0] count down to 0 and VALUE[31:0] will set with RELOAD[31:0] in next EXTIN rising edge. Figure 13.2 and Figure 13.3 are examples for input-edge counter.

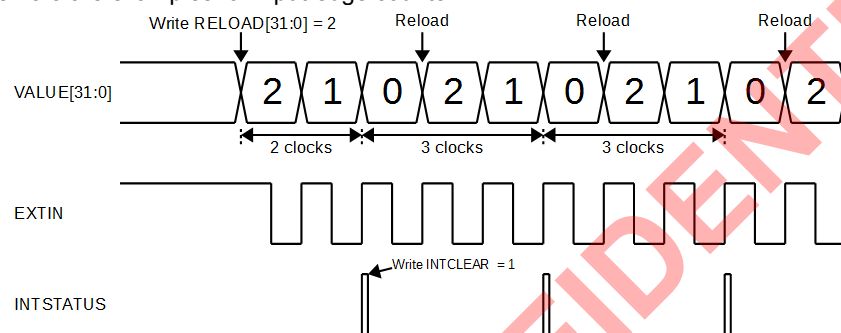


Figure 13.2 A example for input-edge count

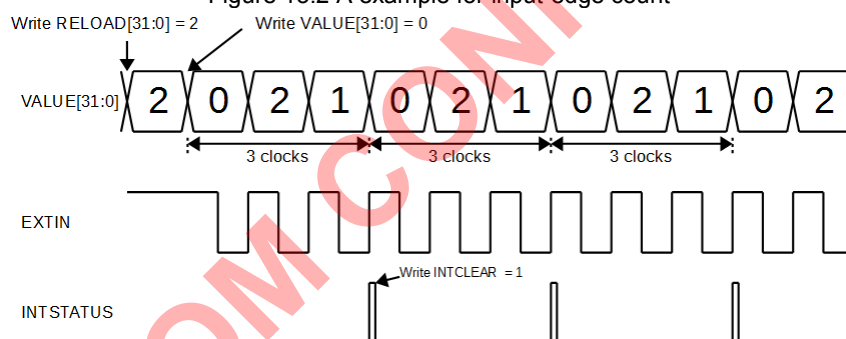


Figure 13.3 Another example for input-edge count

Note: EXTIN must be slower than half of the MCU clock.

13.5.3 Time Capture

When CTRL[1]=1, Timer is in time-capture mode. In this mode, timer will stop count-down when EXTIN=0. User can use this mode to capture time of EXTIN high.

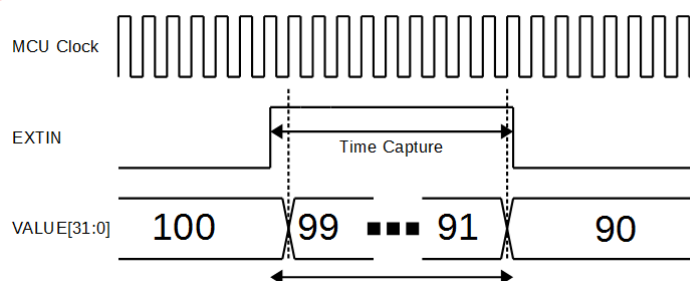


Figure 13.4 A example for time capture

13.5.4 Timer Interrupt

When VALUE[31:0] count-down to 0, the INTSTATUS will set to 1. The interrupt will occur if CTRL[3]=1. User need write INCLEAR=1 to clear INTSTATUS. Please refer Figure 13.2.

The NVIC IRQn of TIMER0 and TIMER1 is 8 and 9. Please refer to Table 11.2 Interrupt Map Vector Table.

Please refer the "SampleCode\A8125M0\Timer" for setup Timer and Timer interrupt.

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14. Dual Timer

Dual Timer is two programmable 16-bits / 32-bits down-counters with MCU clock. Interrupt will generate when any dual timer count-down to 0.

14.1 FEATURE

- Three clock pre-scale: 1, 16, 256
- Two counter sizes: 16-bits and 32-bits
- Three modes: free-running, one-shot and periodic
- One interrupt for two dual timers.
- Background Load

14.2 BLOCK DIAGRAM

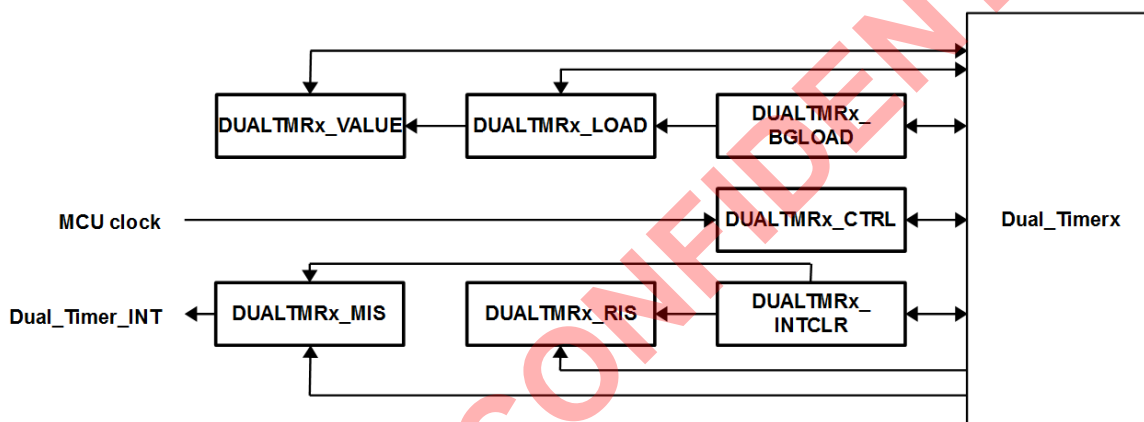


Figure 14.1 Dual Timer block diagram

14.3 REGISTER

14.3.1 Base Address List

Base Address	DESCRIPTION
0x40002000	Dual Timer 1 Base address
0x40002020	Dual Timer 2 Base address

Table 14.1 Base address list

14.3.2 Register List

Offset	Name	DESCRIPTION
0x00	DUALTMRx_LOAD	Dual Timer x Load register
0x04	DUALTMRx_VALUE	Dual Timer x current Value register
0x08	DUALTMRx_CTRL	Dual Timer x Control register
0x0C	DUALTMRx_INTCLR	Dual Timer x Interrupt Clear register
0x10	DUALTMRx_RIS	Dual Timer x Raw Interrupt register
0x14	DUALTMRx_MIS	Dual Timer x Mask Interrupt register
0x18	DUALTMRx_BGLOAD	Dual Timer x Back Ground Load register

Table 14.2 Register list

14.3.3 Register Description

DUALTMRx_LOAD (Dual Timer x Load Register)

Offset: 0x00

R/W	Bit31	-----	Bit 0
W	LOAD[31:0]		
R			
Reset	0x00000000		

LOAD[31:0]: Dual timer x Load value. Write LOAD[31:0] will reset the VALUE[31:0] immediately.

DUALTMRx_VALUE (Dual Timer x current Value Register)

Offset: 0x04

R/W	Bit31	-----	Bit 0
W	VALUE[31:0]		
R			
Reset	0x00000000		

VALUE[31:0]: Dual timer x current count value.

DUALTMRx_CTRL (Dual Timer x Control Register)

Offset: 0x08

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	EN	MD	INTEN	--	PRE[1:0]		SLT	OS
R								
Reset	0	0	1	0	0	0	0	0

EN: Dual timer x Enable

[0]: Disable

[1]: Enable (Dual timer start count down)

MD: Dual timer Mode

[0]: Free-running mode

[1]: Periodic mode

INTEN: Dual timer interrupt enable.

[0]: Dual Timer interrupt disable.

[1]: Dual Timer interrupt enable.

PRE[1:0]: Dual timer prescale.

[00]: Clock is divided by 1.

[01]: Clock is divided by 16

[10]: Clock is divided by 256

[11]: Undefined

SLT: Dual timer size selects 16-bit or 32-bit counter operation

[0]: 16-bit counter

[1]: 32-bit counter

OS: Dual timer one-shot count selects

[0]: Wrapping

[1]: One-shot

DUALTMRx_INTCLR (Dual Timer x Interrupt Clear Register)

Offset: 0x0C

R/W	Bit31	-----	Bit 0
W	INTCLR		
R	--		
Reset	0x00000000		

INTCLR: Timer interrupt clear. Write any value to this register to clean RIS and MIS.

DUALTMRx_RIS (Dual Timer x RIS Register)

Offset: 0x10

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--							--
R								RIS
Reset	0	0	0	0	0	0	0	0

RIS: Dual timer Raw interrupt status.

[0]: VALUE[31:0] not counts down to 0.

[1]: VALUE[31:0] had counted down to 0.

DUALTMRx_MIS (Dual Timer x MIS Register)

Offset: 0x14

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--							--
R								MIS
Reset	0	0	0	0	0	0	0	0

MIS: Dual timer interrupt enabled status from the counter.

[0]: INTEN=0 or RIS=0. Dual Timer interrupt not occur.

[1]: INTEN=1 and RIS=1. Dual Timer interrupt occur.

DUALTMRx_BGLOAD (Dual Timer x Background Load Register)

Offset: 0x18

R/W	Bit31	-----	Bit 0
W	BGLOAD[31:0]		
R			
Reset	0x00000000		

BGLOAD[31:0]: Dual timer Background Load. Write BGLOAD[31:0] will set LOAD[31:0] to BGLOAD[31:0] immediately but not effect to VALUE[31:0].

14.4 FUNCTION DESCRIPTION

14.4.1 Operation Mode

The BIT0 of DUALTMRx_CTRL is OS and the BIT6 of DUALTMR_CTRL is MD. These control bits can set dual timer to three operation mode:

OS	MD	Operation	VALUE reload when counts down to 0
0	0	Free-running	0xFFFF or 0xFFFFFFFF
0	1	Period	LOAD
1	X	One-Shot	Dual Timer Halted. Write LOAD to re-start dual timer.

Table 14.3 Dual Timer operation modes

14.4.2 LOAD and BGLOAD

Dual timer has two reload register: LOAD[31:0] and BGLOAD[31:0]. VALUE[31:0] will be set to LOAD[31:0] when any value write to LOAD[31:0] immediately. LOAD[31:0] will be set to BGLOAD[31:0] when any value write to BGLOAD[31:0] and the same time, VALUE[31:0] will not any effector. Figure 14.2 is an example for write LOAD[31:0] and write BGLOAD[31:0].

Write LOAD[31:0] can modify period and current counting immediately. Write BGLOAD[31:0] can modify period at next time count-down to 0 but does not affect the current counting.

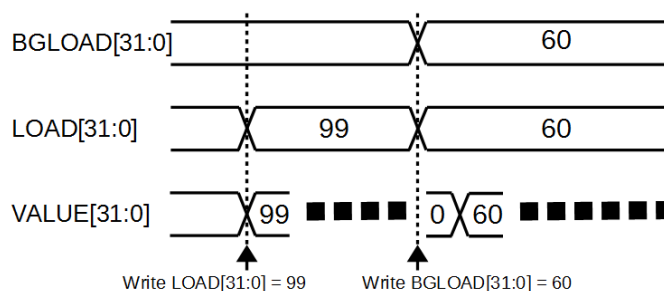


Figure 14.2 An example for write LOAD and BGLOAD

14.4.3 Interrupt

Dual timer 1 and Dual timer 2 have the same interrupt handler. Users can check MIS to distinguish interrupt source. The NVIC IRQn of Dual Timer is 10. Please refer to Table 11.2 Interrupt Map Vector Table.

Interrupt will occurred when VALUE[31:0] count-down to 0 and INTEN=1.

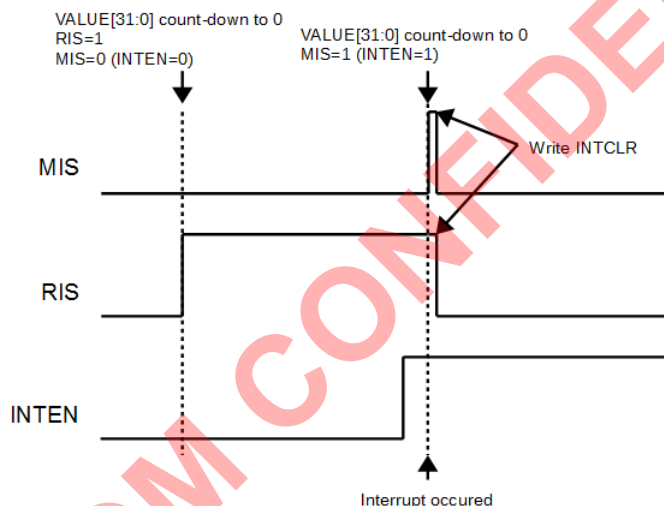


Figure 14.3 Dual Timer interrupt

Please refer the "SampleCode\A8125M0\DualTimer" for setup DualTimer and DualTimer interrupt.

14.4.4 The different between SysTick / Timer0, 1 and Dual Timer

	SysTick	Timer0, Timer1	Dual Timer
Counter clock	MCU clock	MCU clock IO input (can set to counter)	MCU clock
Counter size	24-bits	32-bits	16-bits 32-bits
Interrupt setting	TICKINT=1	Timer0: CTRL[3]=1 and enable NVIC_IRQ8 Timer1: CTRL[3]=1 and enable NVIC_IRQ9	INTEN=1 and enable NVIC_IRQ10
Support Mode	Period	Period	Period Free-running One-shot

Table 14.4 The different between SysTick / Timer0, 1 and Dual Timer

The SysTick is the easiest to use. Most of the timing requirements can be achieved with dual timer. User can choose the timer if need the count or time capture.

15. Watchdog Timer

A8125M0 has a special timer, called Watchdog Timer. It is a useful programmable clock counter that serves as a time-base generator, an event timer or system supervisor. User can use it as a very long timer with disabled reset function.

15.1 FEATURE

- The 32-bit free-running down-counter
- Lock register to prevent accidental write access
- Interrupt and Reset generation

15.2 BLOCK DIAGRAM

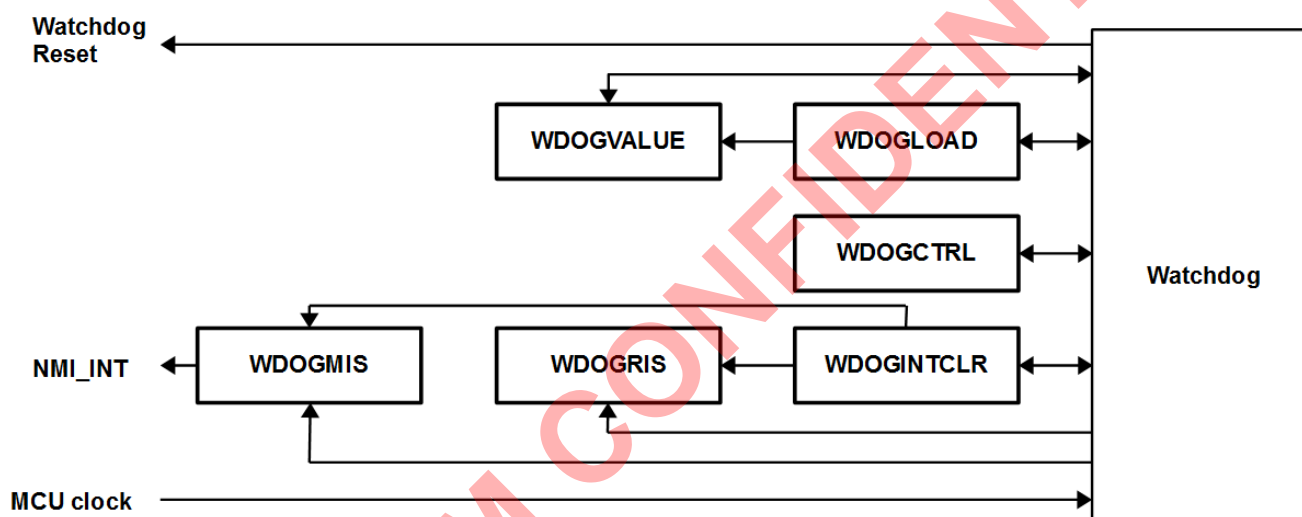


Figure 15.1 Watchdog block diagram

15.3 REGISTER

15.3.1 Register List

Address	Name	DESCRIPTION
0x40008000	WDOGLOAD	Watchdog Load Register
0x40008004	WDOGVALUE	Watchdog Value Register
0x40008008	WDOGCTRL	Watchdog Control Register
0x4000800C	WDOGINTRCLR	Watchdog Interrupt Clean Register
0x40008010	WDOGRIS	Watchdog Raw Interrupt Status Register
0x40008014	WDOGMIS	Watchdog Enabled Interrupt Status Register
0x40008C00	WDOGLOCK	Watchdog Lock Register

Table 15.1 Watchdog register list

15.3.2 Register Description

WDOGLOAD (Watchdog Load Register)

Address: 0x40008000

R/W	Bit 31	-----	Bit 0
W		LOAD[31:0]	
R			
Reset		0xFFFFFFFF	

LOAD [31:0]: The minimum valid value for WDOGLOAD is 1. The watchdog timeout interval is LOAD[31:0] / MCU clock.

WDOGVALUE (Watchdog Value Register)

Address: 0x40008004

R/W	Bit 31	-----	Bit 0
W	VALUE[31:0]		
R	VALUE[31:0]		
Reset	0xFFFFFFFF		

VALUE[31:0]: Current count value

WDOGCTRL (Watchdog CTRL Register)

Address: 0x40008008

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--						RESTEN	INTEN
R	--						RESTEN	INTEN
Reset	0	0	0	0	0	0	0	0

RESTEN: Enable watchdog reset.

[0]: Watchdog reset disable

[1]: Watchdog reset enable

INTEN: Watchdog counter and interrupt enable.

[0]: Disable counter and interrupt

[1]: Enable counter and interrupt

WDOGINTCLR (Watchdog Interrupt Clean Register)

Address: 0x4000800C

R/W	Bit 32	-----	Bit 0
W	INTCLR		
R	INTCLR		
Reset	0x00000000		

INTCLR: A write of any value to clear the watchdog interrupt, and reloads the counter from the value in LOAD.

WDOGRIS (Watchdog RAWINTSTAT Register)

Address: 0x40008010

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--							--
R	--							RAWINTSTAT
Reset	0	0	0	0	0	0	0	0

RAWINTSTAT: Raw Watchdog Interrupt Raw interrupt status from the counter.

WDOGMIS (Watchdog MASKINTSTAT Register)

Address: 0x40008014

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--							--
R	--							MASKINTSTAT
Reset	0	0	0	0	0	0	0	0

MASKINTSTAT: Watchdog Interrupt Enabled interrupt status from the counter.

WDOGLOCK (Watchdog LOCK Register)

Address: 0x40008C00

R/W	Bit31	-----	Bit 0
W	LOCK[31:0]		
R	LOCK[31:0]		
Reset	0x0000 0000		

LOCK: Enable register writes Enable write access to all other registers by writing 0x1ACCE551. Disable write access by writing any other value.

LOCK[0]: Register write enable status

[0]: Write access to all other registers is enabled. (Default)

[1]: Write access to all other registers is disabled.

15.4 FUNCTION DESCRIPTION

15.4.1 Watchdog Interrupt

The interrupt of Watchdog is NMI (Non Maskable Interrupt). It's always working. Please refer to Table 11.1 Exception Types.

Watchdog uses two control bit INTEN and RESTEN. When INTEN=1, the watchdog counter start count-down and interrupt enable. When INTEN=0, the watchdog counter stop count-down and interrupt disable.

RAWINTSTAT=1 when VALUE[31:0] count-down to 0.

MASKINTSTAT=1 when VALUE[31:0] count-down to 0 and RESTEN=1.

15.4.2 Watchdog Reset

Watchdog reset will be occurred when VALUE[31:0] count-down to 0 and MASKINTSTAT=1.

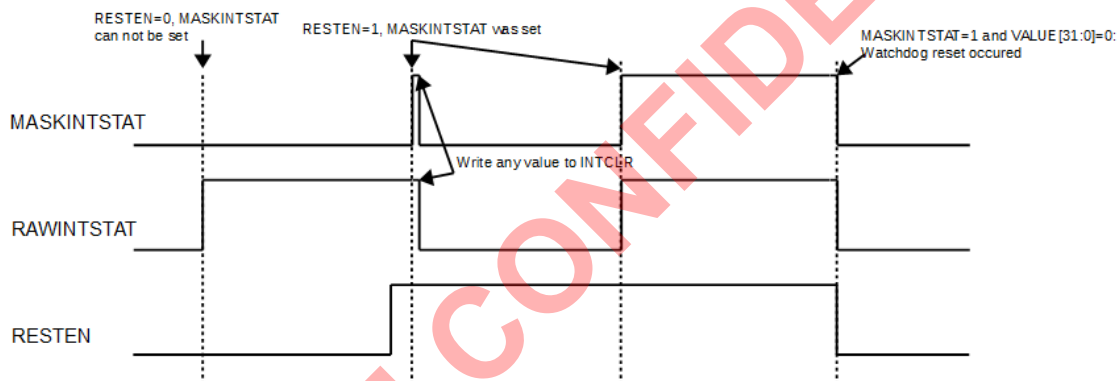


Figure 15.2 A example of watchdog reset

15.5 PROCEDURE

15.5.1 Watchdog Enable

1. Unlock watchdog access, Write 0x1ACCE551 to watchdog lock register
2. Set watchdog load value
3. Enable INTEN=1.
4. Lock watchdog access, Write 0 to watchdog lock register
5. Waiting for watchdog interrupt to occur.
6. Unlock watchdog access, Write 0x1ACCE551 to watchdog lock register.
7. Write 1 to the Watchdog INTCLR register clears the watchdog interrupt, and reloads the counter from the value in watchdog LOAD value.
8. Lock watchdog access, Write 0 to watchdog lock register
9. Repeat step 5~8

15.5.2 Watchdog Reset Enable

1. Unlock watchdog access, Write 0x1ACCE551 to watchdog lock register
2. Set watchdog load value
3. Enable INTEN=1 and RESTEN=1.
4. Lock watchdog access, Write 0 to watchdog lock register
5. Waiting for watchdog interrupt to occur.
6. Unlock watchdog access, Write 0x1ACCE551 to watchdog lock register.
7. Write 1 to the Watchdog INTCLR register clears the watchdog interrupt, and reloads the counter from the value in watchdog LOAD value.
8. Lock watchdog access, Write 0 to watchdog lock register
9. Repeat step 5~8

Watchdog timer that automatically generates a system reset if the main program neglects to periodically service it.

16. PWM

PWM (Pulse Width Modulation) is the method to control analog circuits with a processor's digital outputs. It generates variable pulse frequency and the duty cycle of the signal with digital means. Through PWM function, it can be used for a wide variety of control applications.

16.1 FEATURES

- 8 channels PWM output
- Programmable PWM frequency (1/2, 1/4, 1/8, 1/16, 1/32, 1/64 of MCU clock and that of RTC clock)
- Programmable PWM duty cycle

16.2 PINS DESCRIPTION

PIN	GPIO	TYPE	DESCRIPTION
PWM0	P0_20	OUTPUT	PWM channels 0
PWM1	P0_21	OUTPUT	PWM channels 1
PWM2	P0_10	OUTPUT	PWM channels 2
PWM3	P0_11	OUTPUT	PWM channels 3
PWM4	P0_12	OUTPUT	PWM channels 4
PWM5	P0_13	OUTPUT	PWM channels 5
PWM6	P0_14	OUTPUT	PWM channels 6
PWM7	P0_15	OUTPUT	PWM channels 7

Table 16.1 PWM pins description

16.3 BLOCK DIAGRAM

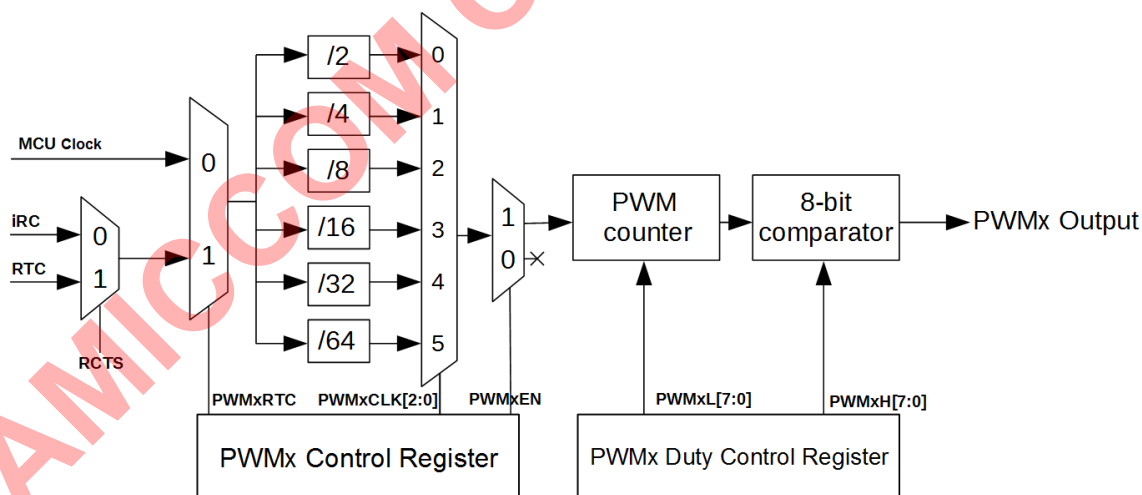


Figure 16.1 PWMx Block Diagram

16.4 REGISTER

16.4.1 Register list

Base Address	DESCRIPTION
0x50004000	PWM0 Base address
0x50004100	PWM1 Base address
0x50004200	PWM2 Base address
0x50004300	PWM3 Base address

Table 16.2 Base address of each PWM

offset	Name	DESCRIPTION
0x000	PWMxCR	PWMx Control Register
0x004	PWMxDCR	PWMx Duty Control Register

Table 16.3 PWM Register List

16.4.2 Register Description

PWMxCR (PWMx Control Register)

Offset: 0x000

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PWMxEN	--			PWMxRTC	PWMxCLK[2:0]		
R								
Reset	0	0	0	0	0	0	0	0

PWMxEN: PWM Channel x Enable,

[0]: Disable.

[1]: Enable.

PWxRTC: PWM Channel x Clock Source select,

[0]: MCU Clock.

[1]: RTC clock.

PWxCLK[2:0]: PWM Channel x Clock select

[000]: PWM Clock / 2

[001]: PWM Clock / 4

[010]: PWM Clock / 8

[011]: PWM Clock / 16

[100]: PWM Clock / 32

[101]: PWM Clock / 64

[110]: Not allowed to use.

[111]: Not allowed to use.

PWMxDCR (PWMx Duty Control Register)

Offset: 0x004

R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	PWMxH [7:0]							
R								
Reset	0	0	0	0	0	0	0	0
R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PWMxL [7:0]							
R								
Reset	0	0	0	0	0	0	0	0

PWMxH[7:0]: PWMx output HIGH register

PWMxL[7:0]: PWMx frequency setting register

16.5 FUNCTION DESCRIPTION

A8125M0 has four channels PWM output. Each channel PWM has an 8-bit counter with comparator, a control register (PWMxCR) and two setting registers (PWMxH and PWMxL). User can select clock source by setting PWMxCR. It divide MCU clock and RTC clock to 2,4,8,16,32,64 by setting PWMxCLK. Enable PWM output and function by setting PWMxEN = 1; otherwise disable PWM output and function by setting PWMxEN = 0. When user sets PWMxEN=1, it outputs LOW single and loads the PWMxL to itself. When the up counter is enabled and matches the content of PWMxH, its output is asserted HIGH; when the counter is overflow, its output is asserted LOW and reload PWMxL to itself. The pulse frequency and the duty cycle for 8-bit PWM is given by the below equations

$$\text{Pulse frequency} = \text{Clock Source} / 2^{(\text{PWMxCLK}+1)} / (256-\text{PWMxL})$$

$$\text{Duty cycle} = (256-\text{PWMxH}) / (256-\text{PWMxL})$$

Noted: PWMxH must be larger than PWMxL. Otherwise, PWM output is always HIGH.
List some example setting in Table 16.4.

MCU Clock = 16MHz RTC Clock = 32.768KHz				
Offset 0x000	Offset 0x004	Clock Source	PWM Frequency	Duty Cycle
0x80	0xFFFFE	16MHz	4MHz	50%
0x80	0xFFFFD	16MHz	2.667KHz	33.3%
0x85	0xFFFFE	16MHz	125KHz	50%
0x80	0x8000	16MHz	31.25KHz	50%
0x88	0x8000	32.768KHz	64Hz	50%
0x88	0xFFFFD	32.768KHz	5.461KHz	33.3%
0x8D	0xFFFFE	32.768KHz	256Hz	50%

Table 16.4 Some example setting

16.6 PROCEDURE

Below is the procedure to set PWM0 output (ex. PWM Frequency 4MHz, Duty Cycle 50%)

- Step1: Set A8125M0 in STBY, PLL, TX or RX MODE.
- Step2: Set Port 0 Output Enable Set Register (0x40010010), P0_20=1.
- Step3: Set Port 0 ALTFUNCSET Register (0x40010018), P0_20=1.
- Step4: Set PWM0CR (0x50004000), PWM0CLK[2:0]=0, and PWM0RTC=0.
- Step5: Set PWM0DCR (0x50004004), PWM0L [7:0]=254, and PWM0H [7:0]=255.
- Step6: Set PWM0CR (0x50004000), PWM0EN=1

PWM0(P0_20) generates 4MHz Pulse frequency and 50% duty cycle of the signal.

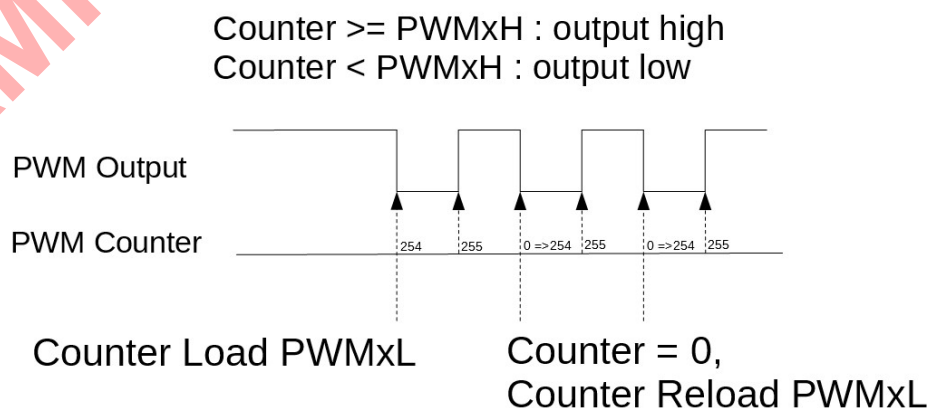
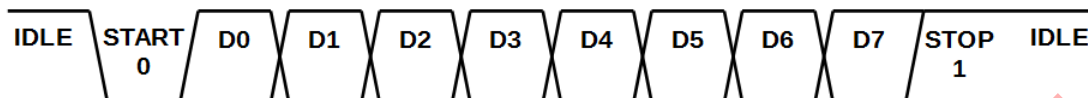


Figure 16.2 An example for PWM

17. UART

The UART implements a universal asynchronous receiver/transmitter function. It supports flexible baudrate generation. It's a simple design that only supports 8-bit communication without parity, and is fixed at one stop bit per configuration (N-8-1).



START: Start bit, always low

D0~D7: Data bit

STOP: Stop bit, always high

Figure 17.1 UART transmission format.

17.1 FEATURE

- Tree UARTs (RX/TX)
- Support format: 8 bit data, 1 start, 1 stop bit and no parities (N-8-1).
- Baud rate derived from system clock.

17.2 PINS DESCRIPTION

PIN	GPIO	TYPE	DESCRIPTION
UART0_RX	P0_16	INPUT	UART0 Receiver Input pin
UART0_TX	P0_17	OUTPUT	UART0 Transmitter Output pin
UART1_RX	P0_18	INPUT	UART1 Receiver Input pin
UART1_TX	P0_19	OUTPUT	UART1 Transmitter Output pin
UART2_RX	P0_20	INPUT	UART2 Receiver Input pin
UART2_TX	P0_21	OUTPUT	UART2 Transmitter Output pin

17.3 BLOCK DIAGRAM

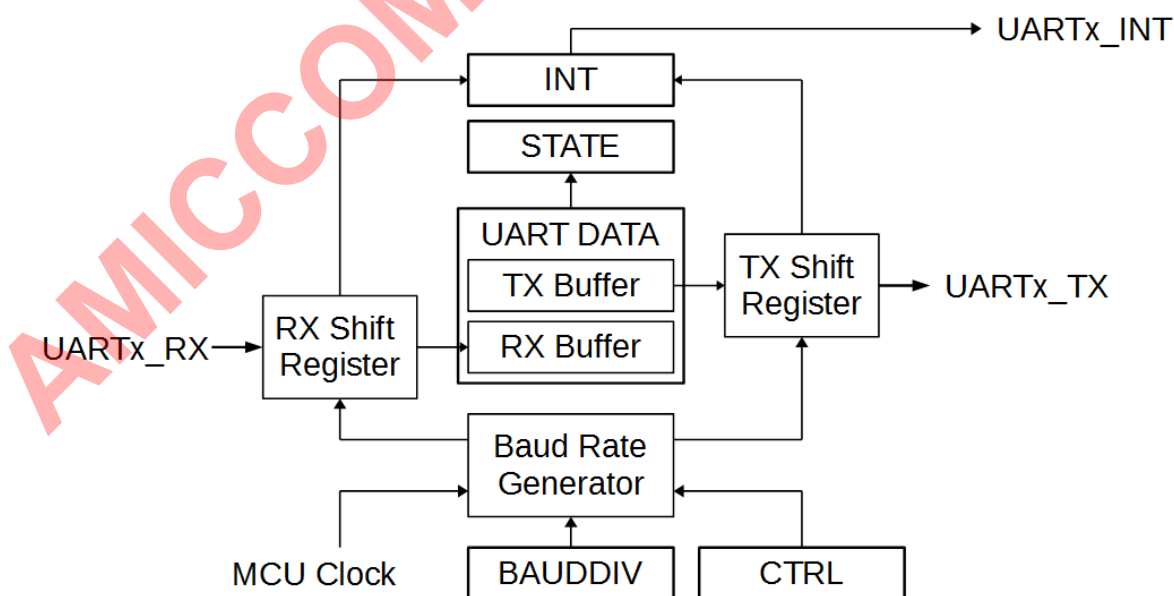


Figure 17.2 UART block diagram

17.4 REGISTER

17.4.1 Base Address List

Base Address	DESCRIPTION
0x40004000	UART0 Base Address
0x40005000	UART1 Base Address
0x40006000	UART2 Base Address

Table 17.1 Base address list

17.4.2 Register List

Offset	Name	DESCRIPTION
0x000	UART_DATA	UART Data Register
0x004	UART_STATE	UART Status Register
0x008	UART_CTRL	UART Control Register
0x00C	UART_INT	UART interrupt state and clear Register
0x010	UART_BAUDDIV	UART Baud rate divider register

Table 17.2 Register list

17.4.3 Register Description

UART_DATA (UART Data Register)

Offset: 0x000

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	DATA[7:0]							
R								
Reset	--	--	--	--	--	--	--	--

DATA[7:0]: UART Data. Write data to TX Buffer or read data from RX Buffer.

UART_STATE (UART Status Register)

Offset: 0x004

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--				STATE[3]	STATE[2]	--	--
R							STATE[1]	STATE[0]
Reset	0	0	0	0	0	0	0	0

STATE[3]: RX buffer overrun.

[0]: RX Buffer does not overrun.

[1]: RX Buffer has overrun. Write 1 to clean this bit.

STATE[2]: TX buffer overrun.

[0]: TX Buffer does not overrun.

[1]: TX Buffer has overrun. Write 1 to clean this bit.

STATE[1]: RX buffer full.

[0]: RX buffer not full.

[1]: RX buffer full.

STATE[0]: TX buffer full.

[0]: TX buffer not full.

[1]: TX buffer full.

UART_CTRL (UART Control Register)

Offset: 0x008

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--		CTRL[5]	CTRL[4]	CTRL[3]	CTRL[2]	CTRL[1]	CTRL[0]
R								
Reset	0	0	0	0	0	0	0	0

CTRL[5] : RX overrun interrupt enable.
[0]: Disable UART RX overrun interrupt.
[1]: Enable UART RX overrun interrupt.

CTRL[4] : TX overrun interrupt enable.
[0]: Disable UART TX overrun interrupt.
[1]: Enable UART TX overrun interrupt.

CTRL[3] : RX interrupt enable.
[0]: Disable UART RX interrupt.
[1]: Enable UART RX interrupt.

CTRL[2] : TX interrupt enable.
[0]: Disable UART TX interrupt.
[1]: Enable UART TX interrupt.

CTRL[1] : RX enable.
[0]: Disable UART RX.
[1]: Enable UART RX.

CTRL[0] : TX enable.
[0]: Disable UART TX.
[1]: Enable UART TX.

UART_INT (UART Interrupt Register)

Offset: 0x00C

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--				INT[3]	INT[2]	INT[1]	INT[0]
R	--				INT[3]	INT[2]	INT[1]	INT[0]
Reset	0	0	0	0	0	0	0	0

INT[3] : RX overrun interrupt.
[0]: RX overrun interrupt does not occur.
[1]: RX overrun interrupt has occurred. Write 1 to clear this bit.

INT[2] : TX overrun interrupt.
[0]: TX overrun interrupt does not occur.
[1]: TX overrun interrupt has occurred. Write 1 to clear this bit.

INT[1] : RX interrupt.
[0]: RX interrupt does not occur.
[1]: RX interrupt has occurred. Write 1 to clear this bit.

INT[0] : TX interrupt.
[0]: TX interrupt does not occur.
[1]: TX interrupt has occurred. Write 1 to clear this bit.

UART_BAUDDIV (UART Baud rate Divider Register)

Offset: 0x010

R/W	Bit 31	-----	Bit 20	Bit 19	-----	Bit 0
W	--			BAUDDIV[19:0]		
R	--			BAUDDIV[19:0]		
Reset	0x000			0x00000		

BAUDDIV[19:0] : Baud rate divider. The minimum number is 16.

17.5 FUNCTION DESCRIPTION

17.5.1 I/O pin setting

To communicate with an external serial interface, the internal UARTx has two external pins known as UARTx_TX and UARTx_RX. The UARTx_TX and UARTx_RX pins are the UARTx transmitter and receiver pins respectively. The UARTx_TX and

UARTx_RX pin function should first be selected by the corresponding pin-shared function selection register (ALTFUNCSET Register) before the UARTx function is used. If set, will automatically setup the UARTx_TX and UARTx_RX pins to their respective TX output and RX input conditions.

17.5.2 UART Baud Rate

The baud rate is depended on MCU clock frequency (**F_{mcu}**), the equation is

$$\text{Baud Rate} = \text{F}_{\text{mcu}} / \text{BAUDDIV}[19:0]$$

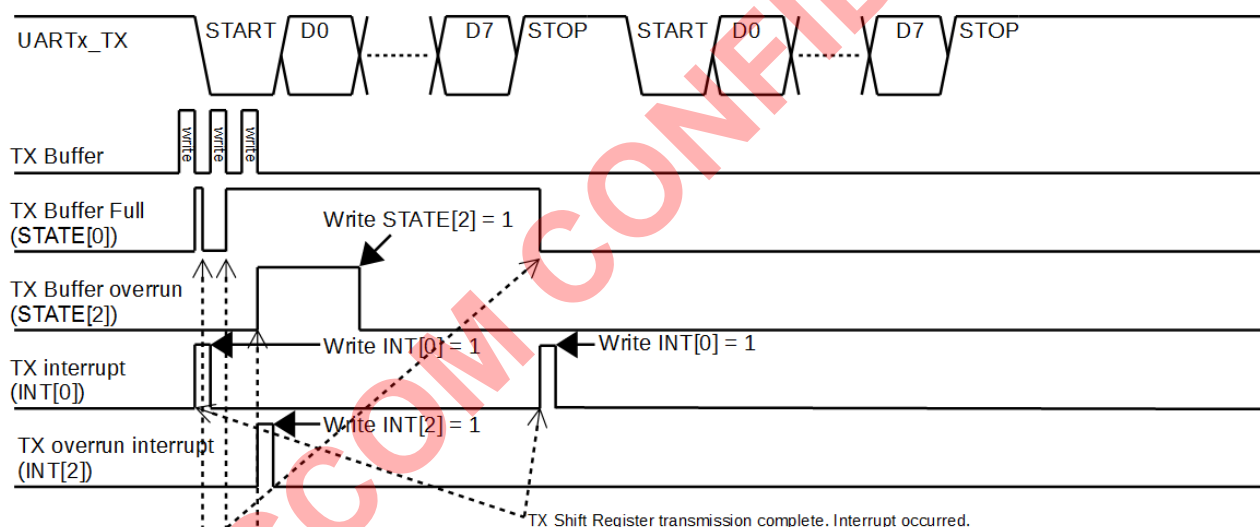
Usually, we choice the baud rate to find the BAUDDIV[19:0]. The equation is

$$\text{BAUDDIV}[19:0] = \text{F}_{\text{mcu}} / (\text{Baud rate})$$

For example, if the system clock frequency is 16MHz and the required baud rate is 9600bps, then the BAUDDIV[19:0] = 16,000,000/9,600 = 1667. And the actual baud rate is 16,000,000/1667 = 9598.08bps (-0.02% with 9600bps).

17.5.3 UART TX state and interrupt

The data of TX Buffer will send to TX Shift Register automatic if TX Shift Register empty. There has 1 data in TX Shift Register to transmit when STATE[0]=0. The STATE[2]=1 when user write data to TX Buffer and STATE[0]=1. INT[0]=1 when TX Shift Register transmit complete.



The data of TX Buffer send to TX Shift Register automatic. STATE[0]=0

TX Shift Register not empty, data hold on TX Buffer. STATE[0]=1

Data can't write to TX Buffer (TX Buffer Full). STATE[2]=1

Figure 17.3 A example for UART TX write 3 bytes data

17.5.4 UART RX state and interrupt

When data send to UARTx_RX, data will store in RX Shift Register. This data will send to RX Buffer automatic when RX Shift Register has received one data. And RX interrupt will occur. User need read data form RX Buffer when STATE[1]=1. If RX Shift Register has received one data and STATE[1]=1 then STATE[3]=1 and data will not send to RX Buffer.

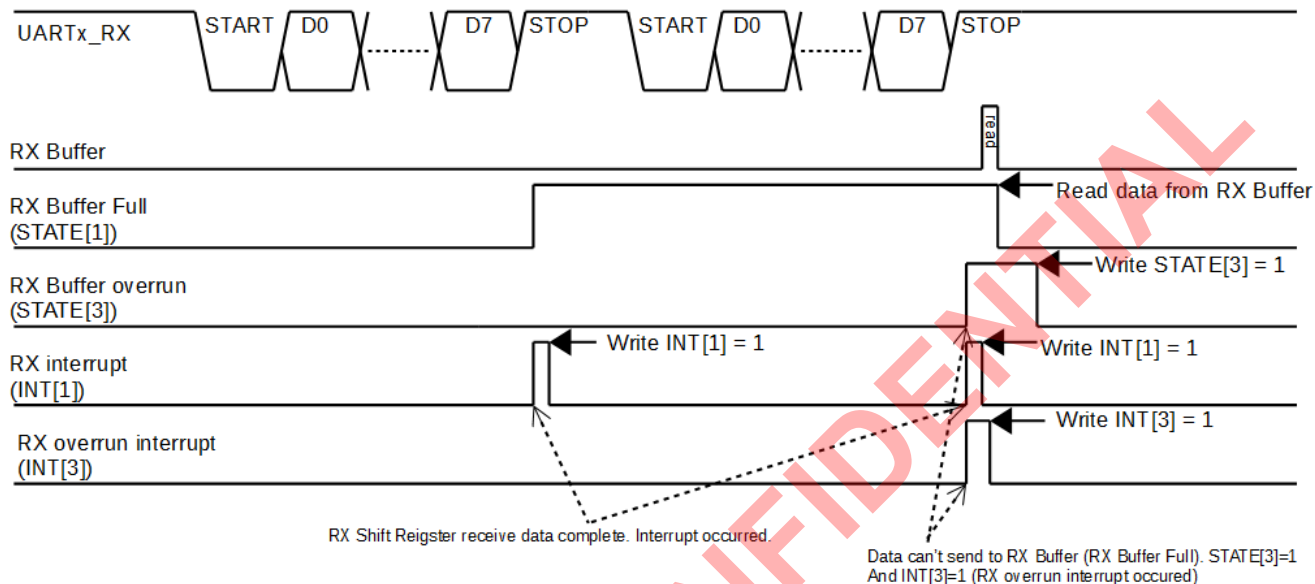


Figure 17.4 A example for UART RX receive data

17.6 PROCEDURE

UARTx TX with interrupt:

1. Set wanted UART I/O port
2. Set Baud Rate.
3. Enable UART TX and enable TX interrupt..
4. Fill in data to UART DATA Register to start transmit data
5. Waiting for TX interrupt to occur and interrupt clear.
6. Repeat step 4~5

UARTx RX with interrupt:

1. Set wanted UART I/O port
2. Set Baud Rate.
3. Enable UART RX and enable RX interrupt..
4. Waiting for RX interrupt to occur and interrupt clear
5. Read out data from UART DATA Register
6. Repeat step 4~5.

Please refer the "SampleCode\A8125M0\UART_INT" for setup UART and UART interrupt.



18.1 FEATURE

- ## 18.2 PINS DESCRIPTION

PIN	GPIO	TYPE	DESCRIPTION
I ² C_SCL	P0_04	INPUT / OUTPUT	I ² C clock input/output
I ² C_SDA	P0_05	INPUT / OUTPUT	I ² C data input/output

18.3 BLOCK DIAGRAM



18.4 REGISTER

18.4.1 Register List

Address	Name	DESCRIPTION
0x50003000	I ² CMSA	I ² C Master Slave Address Register
0x50003004	I ² CMCR / I ² CMSR	I ² C Master Control Register / I ² C Master Status Register
0x50003008	I ² CMBUF	I ² C Master Transmitted/Received data Buffer Register
0x5000300C	I ² CMTP	I ² C Master Timer Period Register
0x50003010	SCL_LP	I ² C_SCL Low Period Register
0x50003014	SCL_HP	I ² C_SCL High Period Register
0x50003018	SDA_SETUP	I ² C_DAT Setup Period Register
0x5000301C	I ² CMINT	I ² C Master Interrupt Register
0x50003804	I ² CSOA	I ² C Slave Own Address Register
0x50003808	I ² CSCR / I ² CSSR	I ² C Slave Control Register / I ² C Slave Status Register
0x5000380C	I ² CSBUF	I ² C Slave Transmitted/Received data Buffer Register
0x50003810	I ² CSOAUP	I ² C Slave Own Address UP Register
0x50003814	I ² CSINT	I ² C Slave Interrupt Register

Table 18.2 I²C interface Register List

18.4.2 I²C Master Register Description

I²CMSA (I²C Master Slave address)

Address: 0x50003000

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	SA[6:0]							RS
R								
Reset	0	0	0	0	0	0	0	0

SA[6:0]: Slave Address.

RS: Receive or Send in START condition. This bit work with START, RUN or HS, RUN.

[0]: Transmitter

[1]: Receiver

I²CMCR (I²C Master Control Register)

Address: 0x50003004

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RSTB	SLRST	--	HS	ACK	STOP	START	RUN
R	--	--	--	--	--	--	--	--
Reset	0	0	0	0	0	0	0	0

RSTB: Reset Bit for I²C Master.

[0]: No effect.

[1]: Reset I²C controller.

SLRST: Slave Reset.

[0]: No effect.

[1]: Reset slaves connected to I²C bus by generating 9 I²C_SCK clocks followed by STOP. This bit need with RUN to work.

HS: Transmission speed switch to High-speed.

[0]: No effect.

[1]: Send START follow by master code and Switching to High-speed.

Please refer the 18.5.2.2 for detail.

ACK: Master in Receive mode need set this bit. This bit must work with RUN bit.

[0]: Read data follow by NAK.

[1]: Read data follow by ACK.

STOP: Send STOP and return to Idle mode, and transmission speed switch to Standard.

[0]: No effect.

[1]: Send STOP.

START: Send START follow by Slave Address and SEND or RECEIVE. This bit need with RUN and RS to work.

[0]: No effect.

[1]: Send START follow by Slave Address and SEND or RECEIVE.

RUN: This bit work with START, STOP, ACK and HS.

[0]: No effect.

[1]: Run a transmission.

I²CMSR (I²C Master Status Register)

Address: 0x50003004

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--	--	--	--	--	--	--	--
R	--	BUS_BUSY	IDLE	ARB_LOST	DATA_ACK	--	ERROR	BUSY
Reset	0	0	1	0	0	0	0	0

BUS_BUSY: This bit is set by START conditions and reset by STOP conditions.

[0]: Bus not busy.

[1]: Bus is busy.

IDLE: I²C Bus controller is in the idle state.

[0]: I²C Bus controller is not in idle state.

[1]: I²C Bus controller is in idle state.

ARB_LOST: Due to the last operation I²C Bus controller lost the arbitration.

[0]: not arbitration lost.

[1]: has arbitration lost.

DATA_ACK: The acknowledged of DATA.

[0]: DATA with NAK.

[1]: DATA with ACK.

ERROR: Due to the last operation an error occurred, including slave address wasn't acknowledged, transmitted data wasn't acknowledged, or I²C Bus controller lost the arbitration.

[0]: Normal.

[1]: Some error occurred.

BUSY: I²C Master is receiving, or transmitting data on the bus and other bits of I²CMSR are no valid.

[0]: I²C Master controller not busy.

[1]: I²C Master controller is busy.

I²CMBUF (I²C Master Transmitted/Received data Buffer)

Address: 0x50003008

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	D[7:0]							
R								
Reset	0	0	0	0	0	0	0	0

D[7:0]: I²C Master write SEND data or read RECEIVE data.

I²CMTP (I²C Master Timer Period)

Address: 0x5000300C

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	0	MTP[6:0]						
R	0							
Reset	0	0	0	0	0	0	0	1

MTP[6:0]: I²C master timer period register. The range of MTP[6:0] is 1~63

SCL_LP (I²C_SCL Low Period)

Address: 0x50003010

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--				SCL_LP[3:0]			
R	--				SCL_LP[3:0]			
Reset	0	0	0	0	0	1	0	0

SCL_LP[3:0]: I²C master SCL low time period register. The range of SCL_LP[3:0] is 2~15

SCL_HP (I²C_SCL High Period)

Address: 0x50003014

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--				SCL_HP[3:0]			
R	--				SCL_HP[3:0]			
Reset	0	0	0	0	0	0	1	0

SCL_HP[3:0]: I²C master SCL high time period register. The range of SCL_HP[3:0] is 2~15

SDA_SETUP (I²C_DAT Setup Period)

Address: 0x50003018

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--				SDA_SETUP[3:0]			
R	--				SDA_SETUP[3:0]			
Reset	0	0	0	0	0	0	1	0

SDA_SETUP[3:0]: I²C Master SDA setup time register. The range of SDA_SETUP[3:0] is 1~14.

I²CMINT (I²C Master Interrupt)

Address: 0x5000301C

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--						I ² CMIF	I ² CMIE
R	--						I ² CMIF	I ² CMIE
Reset	0	0	0	0	0	0	0	0

I²CMIF: I²C MASTER MODULE interrupt flag

[0]: No effect.

[1]: I²C Master Interrupt occurred. Write 1 to clean this bit.

I²CMIE: I²C Master interrupt enable

[0]: Disable.

[1]: Enable.

18.4.3 I²C Slave Register Description

I²CSOA (I²C Slave Own Address)

Address: 0x50003804

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	ADDR[6:0]							
R	ADDR[6:0]							
Reset	0	0	0	0	0	0	0	0

ADDR[6:0]: Slave device 7bits own address.

I²CSCR (I²C Slave Control Register)

Address: 0x50003808

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RSTB	DA	--	--	RECFINCLR	SENDFINCLR	--	--
R	--	--	--	--	--	--	--	--
Reset	0	0	0	0	0	0	0	0

RSTB: I²C Slave controller reset.

[0]: No effect.

[1]: Reset I²C Slave controller.

DA: I²C module Device Active.

[0]: I²C Slave device inactive.

[1]: I²C Slave device active.

RECFINCLR: RECFIN clear.

[0]: No effect.

[1]: Clear RECFIN flag.

SENDFINCLR:

[0]: No effect.

[1]: Clear SENDFIN flag.

I²CSSR (I²C Slave Status Register)

Address: 0x50003808

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--	--	--	--	--	--	--	--
R	--	DA	--	BUSACTIVE	RECFIN	SENDFIN	TREQ	RREQ
Reset	0	0	0	0	0	0	0	0

DA: I²C slave Device Active.

[0]: I²C slave device inactive.

[1]: I²C slave device active.

BUSACTIVE: BUS ACTIVE

[0]: Bus no any transmission.

[1]: Bus has any transmission.

RECFIN: Receive Finish.

[0]: No effect.

[1]: I²C Slave device receive finish. User need write 1 to RECFINCLR to clear this bit.

SENDFIN: Send Finish.

[0]: No effect.

[1]: I²C Slave device send finish. User need write 1 to SENDFINCLR to clear this bit.

TREQ: Transmit Request.

[0]: No transmit request.

[1]: I²C Slave device is addressed as transmitter and requires data from host. User need write data to I²C Slave Transmitted/Received data buffer (0x5000380C) to clear this bit.

RREQ: Receive Request

[0]: No receive request.

[1]: Receive request occurred. User need read data from I2CSBUF to clear this bit.

I²CSBUF (I²C Slave Transmitted/Received data Buffer)

Address: 0x5000380C

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	D[7:0]							
R								
Reset	0	0	0	0	0	0	0	0

D[7:0]: I²C Slave read data from D[7:0] when RREQ occurred. And write data to D[7:0] when TREQ occurred.

I²CSOAUP (I²C Salve Own Address UP)

Address: 0x50003810

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W					TEN_ADDR_EN	ADDR[9:7]		
R	--							
Reset	0	0	0	0	0	0	0	0

TEN_ADDR_EN: Ten bits address enable.

[0]: I²C Slave device using 7bits address.

[1]: I²C Slave device using 10bits address.

ADDR[9:7]: The higher 3 bits for I²C Slave device 10bits own address.

I²CSINT (I²C Slave Interrupt register)

Address: 0x50003814

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W							I ² CSIF	I ² CSIE
R	--							
Reset	0	0	0	0	0	0	0	0

I²CSIF: I²C Slave device interrupt flag.

[0]: No effect.

[1]: I²C Slave device interrupt occurred. Write 1 to clear this bit.

I²CSIE: I²C Slave device interrupt enable.

[0]: Disable.

[1]: Enable.

18.5 FUNCTION DESCRIPTION

18.5.1 I²C Transmission Format

I²C transmission uses 2 signals: I²C_SCL and I²C_SDA. The transmission format consists of START, STOP, DATA and Acknowledge. These 2 signals are the open-drain signal, therefore, they need to use resistor to pull high. The resistor value is determined by transmission speed and circuit design. In general, 4.7Kohm can be used when transmission speed is 400Kbps.

When I²C_SCL is high, I²C_SDA is changed from high to low, it is called START.

When I²C_SCL is high, I²C_SDA is changed from low to high, it is called STOP.

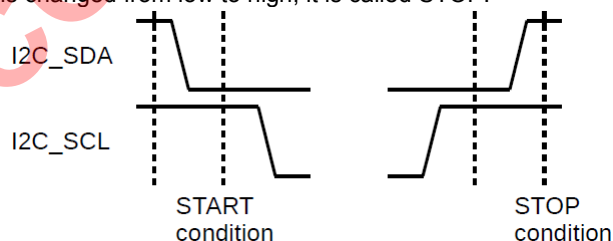


Figure 18.2 START condition and STOP condition

DATA is fixed to 8 bits. When data is sent, I²C_SDA can be changed state only I²C_SCL is low. After each 8 bits DATA is sent, 1 bit Acknowledge should be followed. It is called ACK when Acknowledge=0. It is called NAK when Acknowledge=1:

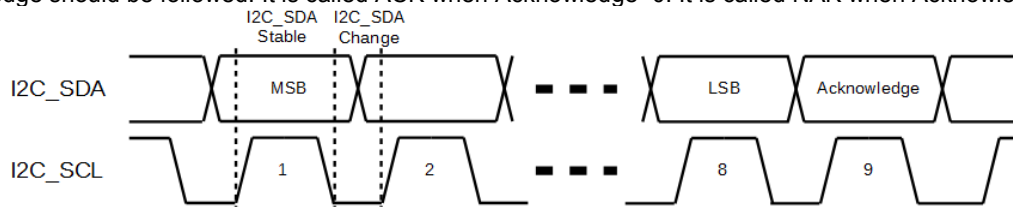


Figure 18.3 Data Validity

I²C Bus must be checked and it is idle before sending. When I²C bus is idle, START can be sent by I²C Master. I²C bus will be occupied after sending START and the other I²C host will be not transmitted. I²C Bus will be released and changed to idle until STOP is sent. The simplest data and successful data of an I²C transmission will contain START, SA [7: 0], RS, Acknowledge (0), DATA [7: 0], Acknowledge, STOP at least. Please refer following figure:

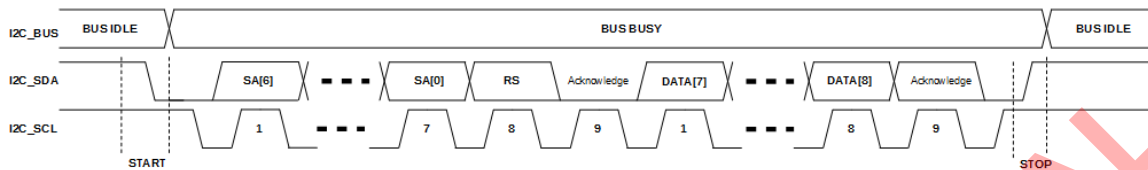


Figure 18.4 A simple I²C Transmission

For easy to describe, these symbols will be used later.

- S represents START.
- Sr represents Repeat START.
- a represents Acknowledge to send by device (slave). The a is include 0 (ACK) and 1 (NAK).
- A represents Acknowledge to send by I²C Master. The A is include 0 (ACK) and 1 (NAK).
- P represents STOP.
- RS represents the receive/send bit. RS is include the 0 (send) and 1 (receive).

After sending START, then slave address and RS will be transmitted. If address of I²C Bus matched with device, I²C_SDA will be pulled low and generated ACK by device, transmission will be continued.

S 7 bits Slave Address RS 0

If I²C bus does not match with device, I²C_SDA keeps high and generated NAK. STOP will be transmitted by I²C Master and transmission will be ended.

S 7 bits Slave Address RS 1 P

It represents I²C Master to send data to device when RS is 0.

S 7 bits Slave Address 0 0 8 bits data SEND a

ACK will be returned when Device received data normally. STOP will be sent by I²C Master to release I²C Bus when transmission was ended.

8 bits data SEND 0 --- 8 bits data SEND 0 P

NAK will be returned when Device cannot receive data or error happened. In general, STOP will be sent by I²C Master to release I²C Bus.

8 bits data SEND 1 P

It represents device sends data to I²C Master when RS is 1.

S 7 bits Slave Address 1 0 8 bits data RECEIVE A

In general, ACK will be set when I²C Master keeps receiving data. NAK will be set and STOP will be sent for transmission ending when I²C Master does not receive data.

8 bits data RECEIVE 0 --- 8 bits data RECEIVE 1 P

During transmission, if the I²C Master wants to change the transmission direction or with other Device to communicate, and does not want to release I²C BUS. START is sent again when STOP does not send. The START is called Repeat START. Transmission will be continued after Repeat START.

To use Repeat START read data (RS=1) from Device after I²C Master sending data.

--- 8 bits data SEND a Sr 7 bits Slave Address 1 a 8 bits data RECEIVE A ---

To use Repeat START send data (RS=0) to Device after I²C Master reading data.

--- 8 bits data RECEIVE 0 Sr 7 bits Slave Address 0 a 8 bits data SEND a ---

Via combine these formats, I²C transmission can be completed.

18.5.2 I²C Transmission Speed

A lot of transmission speed is defined by I²C protocol, including

- Standard Mode (<= 100K bps)
- Fast Mode (<= 400 Kbps)
- Fast Mode Plus (<= 1M bps)
- High Speed Mode (<= 3.4 Mbps)

Standard mode, fast mode and fast mode plus do not require extra control. The high speed mode requires a specific Master Code to control

18.5.2.1 Normal Speed

In Normal Speed, I²C Master supports these transmission speed : Standard Mode (<= 100K bps), Fast Mode (<= 400 Kbps) and Faster Mode Plus (<= 1M bps) of I²C. MTP[6:0] (0x5000300C), SCL_LP[3:0] (0x50003010) and SCL_HP[3:0] (0x50003014) can be combined transmission speed wanted by user. The formula is as follows:

$$\text{SCL_PERIOD} = 2 \times (1 + \text{MTP}[6:0]) \times (\text{SCL_LP}[3:0] + \text{SCL_HP}[3:0]) \times \text{CLK_PRD}$$

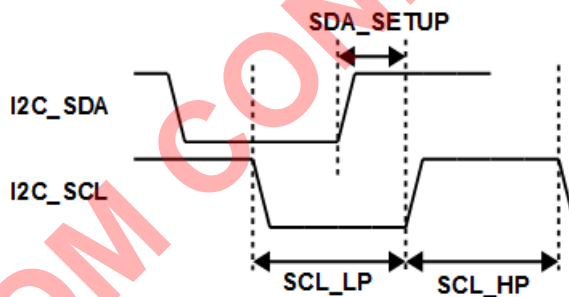
$$\text{SCL_FREQUENCY} = 1 / \text{SCL_PERIOD}$$

For example, if CLK_FRQ = 16MHz, CLK_PRD = 62.5ns. MTP[6:0] = 3, SCL_LP[3:0] = 6, SCL_HP[3:0] = 4.
Then SCL_PERIOD = 2 x (1 + 3) x (6 + 4) x 62.5ns = 5000ns = 5us
And SCL_FREQUENCY = 1 / 5us = 200 KHz

SCL_LP [3:0] is used to determine the duration of I²C_SCL at low.

SCL_HP[3:0] is used to determine the duration of I²C_SCL at high.

SDA_SETUP [3: 0] is used to determine the time point of I²C_SDA conversion. SDA_SETUP[3:0] need less than SCL_LP[3:0].



NOTE: SCL_LP > SDA_SETUP

Figure 18.5 SCL_LP, SCL_HP and SDA_SETUP

18.5.2.2 High Speed

When Device supports High Speed Mode, Master Code (0b00001XXX) can be sent after START, followed a forced NAK Acknowledge. And then, Speed will be changed to High Speed. High Speed will be back to Normal Speed until transmission end.

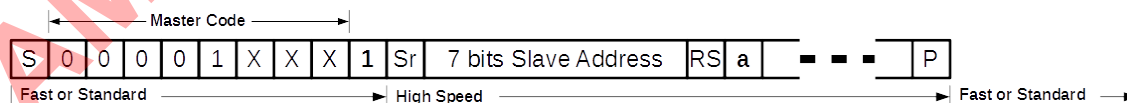


Figure 18.6 Switch to High Speed Mode until STOP

Please be noted, the Master Code is provided by the Device that supports High Speed Mode.

In I²C Master, bit HS controls whether to enter the High Speed Mode or not. Transmission speed of High Speed Mode is fixed (MTP=1, SCL_LP=2, SCL_HP=1, SDA_SETUP=1) as follows:

$$\text{SCL_PERIOD} = 12 \times \text{CLK_PRD}$$

$$\text{SCL_FREQUENCY} = \text{MCU Clock} / 12$$

User can follow as below:

Step1: I²CMSA (0x50003000) = Master Code

Step2: I²CMCR (0x50003004) = 0x13 (HS=1, START=1, RUN=1)

Step3: Wait BUSY bit of I²CMSR (0x50003004) from 1 to 0. The speed is switch to high speed until STOP occurred.

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18.5.3 I²C Master

I²C Master will be switched at Idle State, Master Transmitter and Master Receiver.

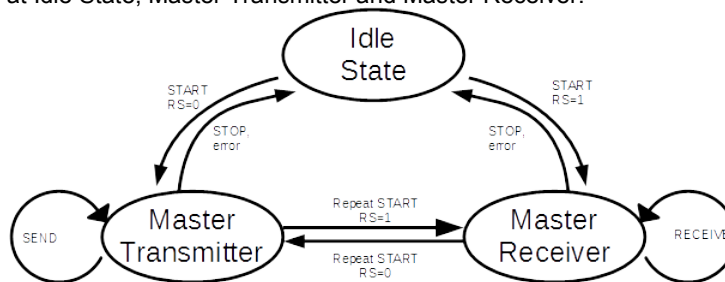


Figure 18.7 State of I²C Master

18.5.3.1 I²C Master Control

I²C Master can control by the main use of I²CMSA (0x50003000) and I²CMCR (0x50003004). Bit RS is included in I²CMSA. These bits RSTB, SLRST, HS, ACK, STOP, START and RUN are included in I²CMCR. These control bits can be combined the following transmission formats:

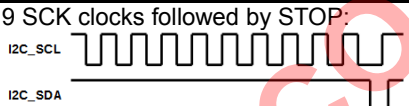
R S	R S T B	S L R S T	H S	A C K	S T O P	S T A R T	R U N	OPERATION	Next I ² C Master State	Next Speed Mode
X	1	0	X	X	X	X	X	I ² CM module software reset	Idle	Normal
0	0	1	0	0	0	0	1	9 SCK clocks followed by STOP: 	Idle	Normal
0	0	0	0	X	0	1	1	S 7 bits Slave Address 0 a 8 bits data SEND a	Transmitter	Continue
0	0	0	0	X	1	1	1	S 7 bits Slave Address 0 a 8 bits data SEND a P	Idle	Normal
1	0	0	0	0	0	1	1	Sr 7 bits Slave Address 1 a 8 bits data RECEIVE 1	Receiver	Continue
1	0	0	0	0	1	1	1	Sr 7 bits Slave Address 1 a 8 bits data RECEIVE 1 P	Idle	Normal
1	0	0	0	1	0	1	1	Sr 7 bits Slave Address 1 a 8 bits data RECEIVE 0	Receiver	Continue
0	0	0	1	0	0	0	1	S Master Code 0 a	Transmitter	High Speed

Table 18.3 Control bits combinations permitted in Idle state

R S	R S T B	S L R S T	H S	A C K	S T O P	S T A R T	R U N	OPERATION	Next I ² C Master State	Next Speed Mode
X	1	0	X	X	X	X	X	I ² CM module software reset	Idle	Normal
X	0	0	0	X	1	0	0	P	Idle	Normal
X	0	0	0	X	0	0	1	8 bits data SEND a	Transmitter	Continue
X	0	0	0	X	1	0	1	8 bits data SEND a P	Idle	Normal
0	0	0	0	X	0	1	1	Sr 7 bits Slave Address 0 a 8 bits data SEND a	Transmitter	Continue
0	0	0	0	X	1	1	1	Sr 7 bits Slave Address 0 a 8 bits data SEND a P	Idle	Normal
1	0	0	0	0	0	1	1	Sr 7 bits Slave Address 1 a 8 bits data RECEIVE 1	Receiver	Continue
1	0	0	0	0	1	1	1	Sr 7 bits Slave Address 1 a 8 bits data RECEIVE 1 P	Idle	Normal
1	0	0	0	1	0	1	1	Sr 7 bits Slave Address 1 a 8 bits data RECEIVE 0	Receiver	Continue

Table 18.4 Control bits combinations permitted in Master Transmitter

R	S	R	S	S	H	A	S	S	R	OPERATION	Next I ² C Master State	Next Speed Mode
S	T	L	S	C	T	O	T	U	N			
B	B	S		K	O	P	R	N				
T	T	T										
X	1	0	X	X	X	X	X	X		I ² CM module software reset	Idle	Normal
X	0	0	0	X	1	0	0		P		Idle	Normal
X	0	0	0	0	0	0	0	1		8 bits data RECEIVE 1	Receiver	Continue
X	0	0	0	0	1	0	1		P		Idle	Normal
X	0	0	0	1	0	0	1			8 bits data RECEIVE 0	Receiver	Continue
1	0	0	0	0	0	1	1	S		7 bits Slave Address 1 a 8 bits data RECEIVE 1	Receiver	Continue
1	0	0	0	0	1	1	1	S		7 bits Slave Address 1 a 8 bits data RECEIVE 1 P	Idle	Normal
1	0	0	0	1	0	1	1	S		7 bits Slave Address 1 0 8 bits data RECEIVE 0	Receiver	Continue
0	0	0	0	X	0	1	1	Sr		7 bits Slave Address 0 a 8 bits data SEND a	Transmitter	Continue
0	0	0	0	X	1	1	1	Sr		7 bits Slave Address 0 a 8 bits data SEND a P	Idle	Normal

Table 18.5 Control bits combinations permitted in Master Receiver

18.5.3.2 BUSY bit

When Control bit write to I²CMCR, the BUSY bit will not change to high immediately. There are about delay 2us.

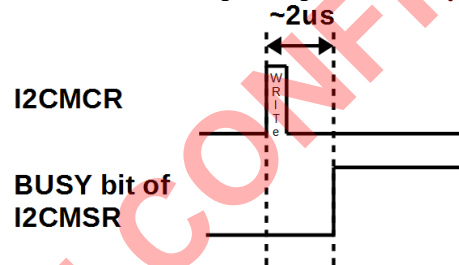


Figure 18.8 Timing for BUSY bit

18.5.3.3 I²C Master Interrupt

To use the I²C Master interrupt, in addition to set I²CMIE = 1 in I²CMINT (0x5000301C), I²C_INT=1 should be set in NVIC. Please refer to Table 11.2 Interrupt Map Vector Table.

When any transmission is completed by I²C Master, I²C Master Interrupt will be generated. I²CMIF can be determined whether interrupt is generated by I²C Master.

User need write I²CMIF=1 to clean I²CMIF.

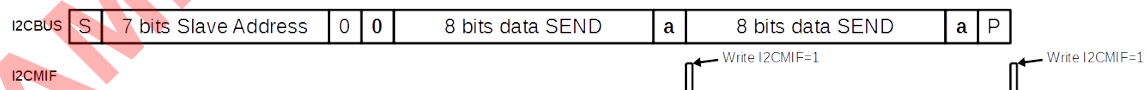


Figure 18.9 I²CMIF=1 when transmit finish

18.5.3.4 I²C Master Transmit

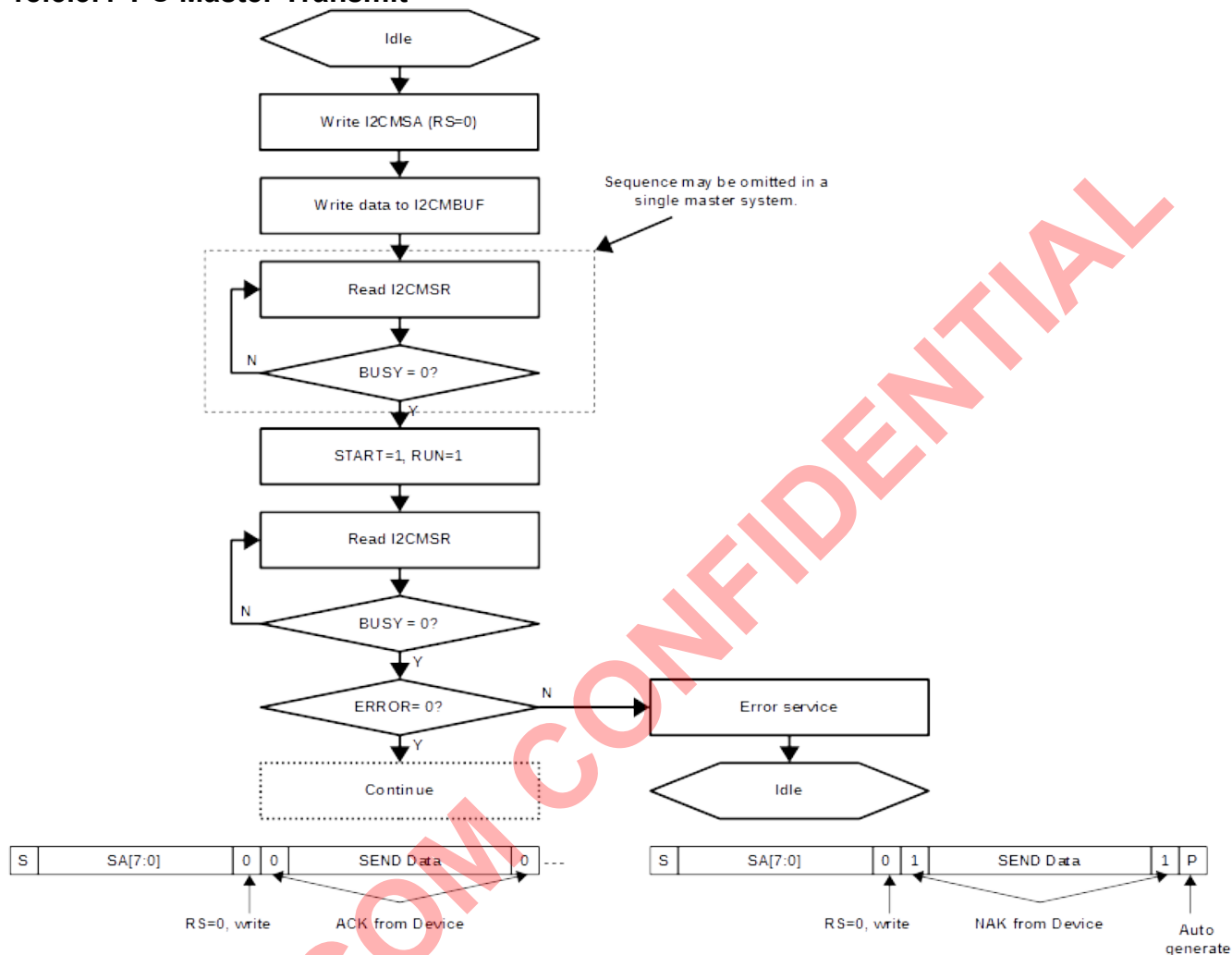


Figure 18.10 The flow chart of I²C Master Transmit

18.5.3.5 I²C Master Receive

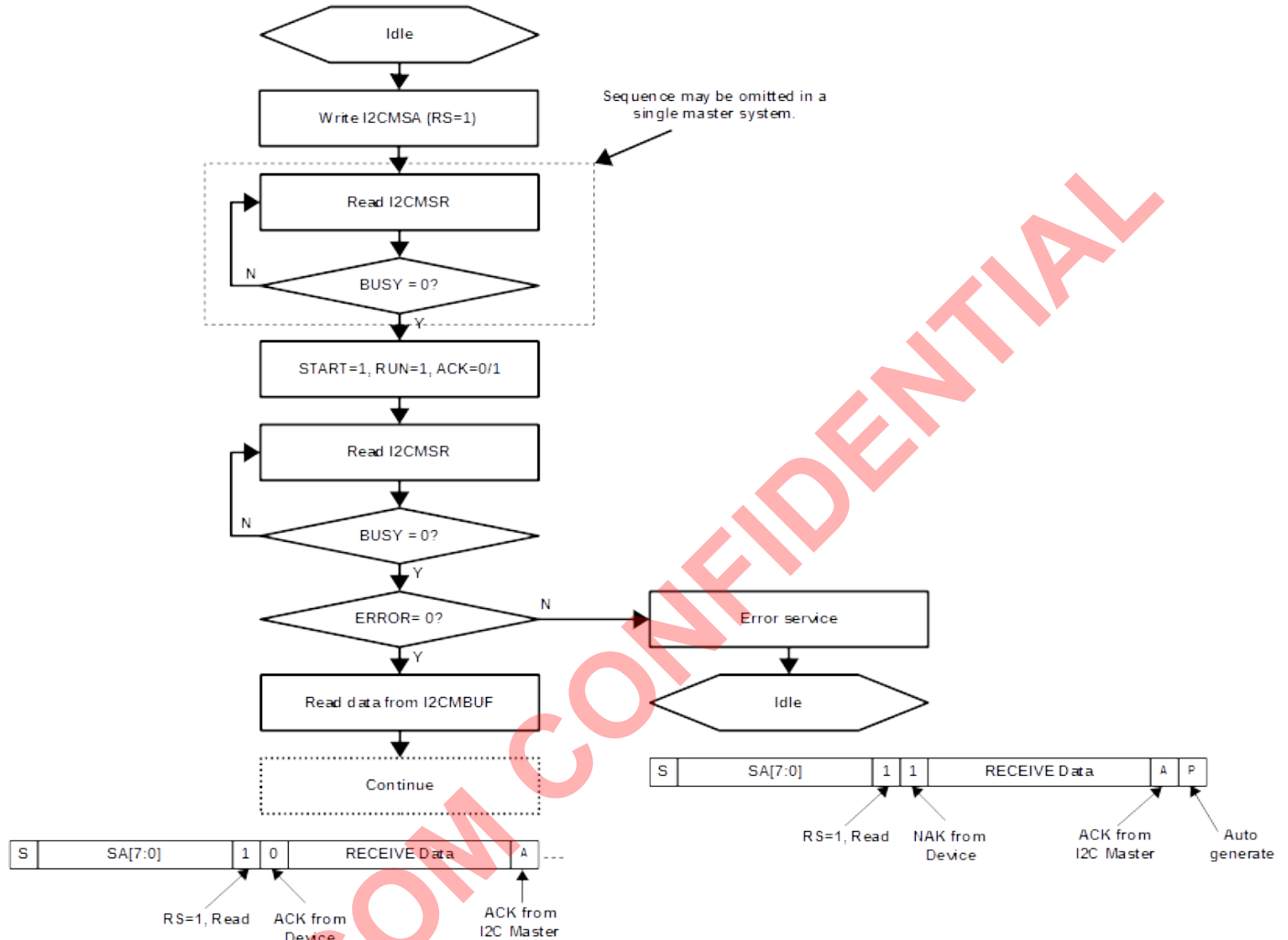


Figure 18.11 The flow chart of I²C Master Receive

18.5.3.6 I²C Master Transmit with Repeat START

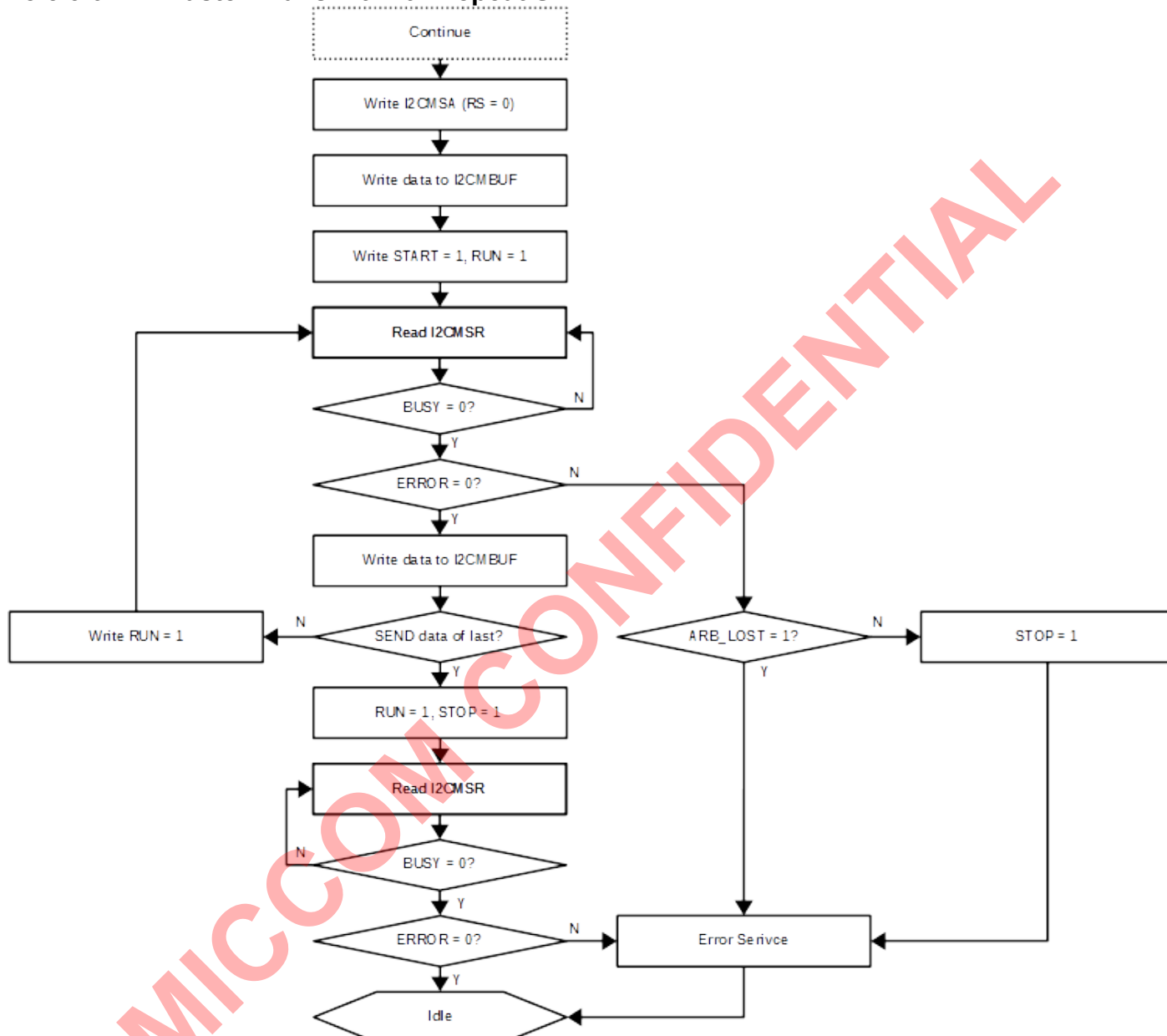


Figure 18.12 The flow chart of I²C Master Transmit with Repeat START

18.5.3.7 I²C Master Receive with Repeat START

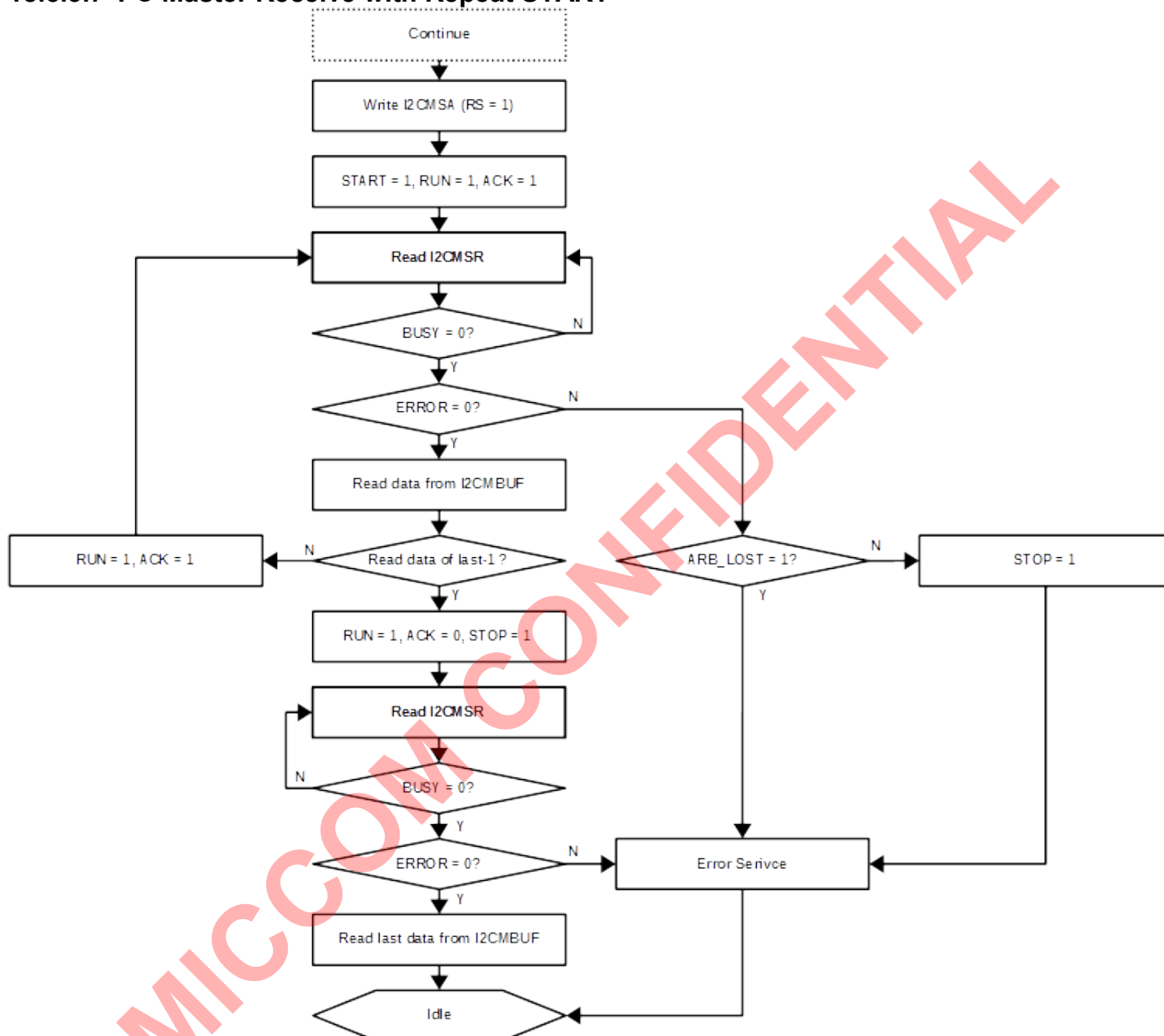


Figure 18.13 The flow chart of I²C Master Receive with Repeat START

18.5.4 I²C Slave

I²C Slave will be switched at Idle State, Slave Receiver and Slave Transmitter.

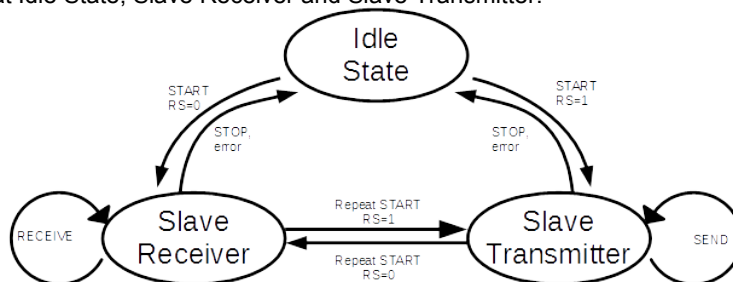


Figure 18.14 State of I²C Slave

18.5.4.1 I²C Slave Control

Because I²C Slave can only be received state passively, therefore, bits need to be controlled less actually. I²C Slave will be ready when after set DA=1. And then, read the state of the I²CSSR to determine the action.

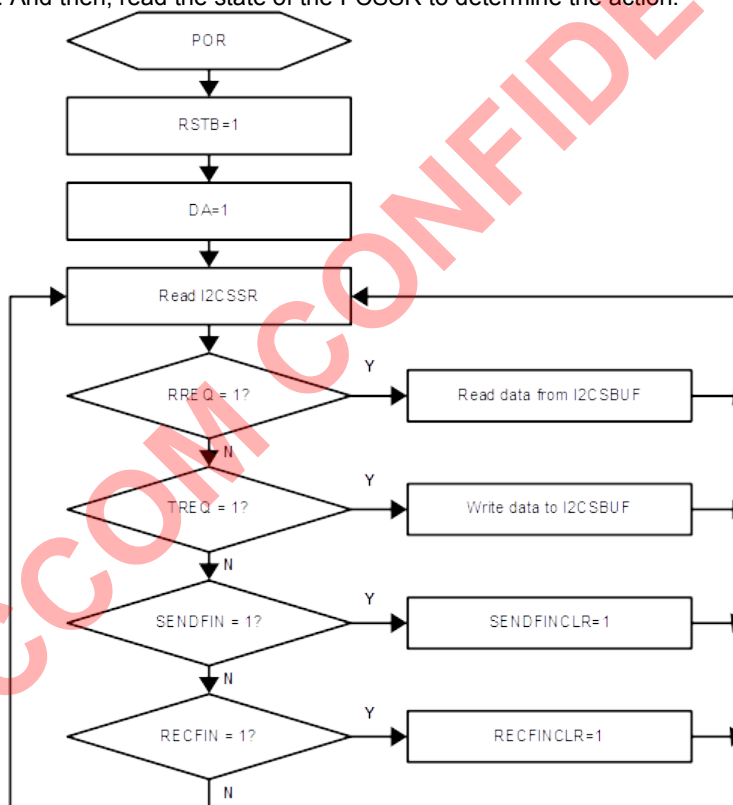


Figure 18.15 The flow chart of I²C Slave

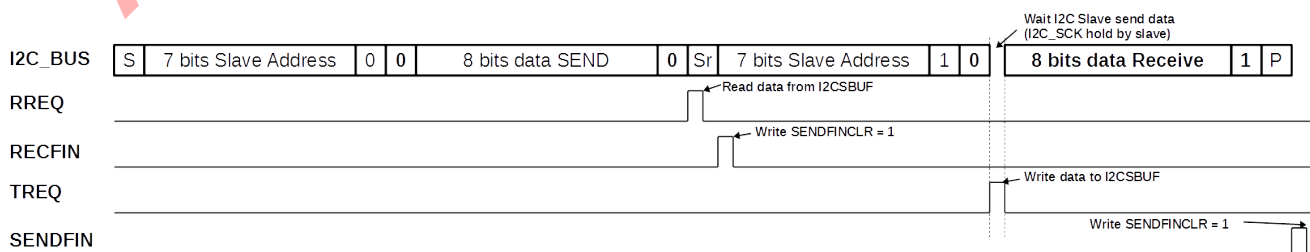


Figure 18.16 Timing for RREQ, TREQ, RECFIN, SENDFIN

18.5.4.2 I²C Slave Interrupt

To use the I²C Slave interrupt, in addition to set I²CSIF=1 in I²CSINT (0x50003814), I²C_INT=1 should be set in NVIC. Please Refer to Table 11.2 Interrupt Map Vector Table.

When any signal of RREQ or TREQ or SENDFIN or RECFIN is generated by I²C Slave, I²C Slave interrupt will be generated. I²CSIF can be determined whether interrupt is generated by I²C Slave. After interrupt generation, I²CSIF should be written to 1 to clear I²CSIF.

18.5.5 10 Bit Address

I²C protocol uses 10 Bit Address to solve address 7 Bit Address caused by the lack of address space, and it can be compatible with the original 7 Bit Address protocol. Preamble “11110” is used to determine 10 Bit Address and 7 Bit Address by 10 Bit Address. Followed by 2 Bits Slave Address (SA [9: 8]), and then the next packet can be written to the remaining 8 Bits Slave Address (SA [7: 0]).

The following format is used to write and read 10 Bit Address Device generally:

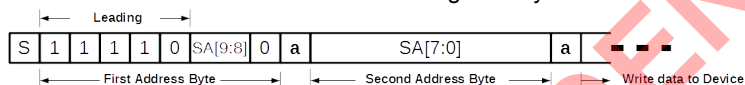


Figure 18.17 Write data to 10 Bit Address Device

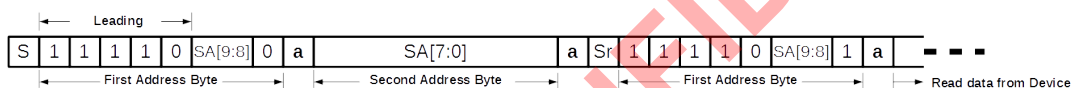


Figure 18.18 Read data from 10 Bit Address Device (It needs to use Repeat Start to direction conversion).

18.5.5.1 10 Bit Address for I²C Master

Because 10 Bit Address is compatible with 7 Bit Address, I²C Master does not need to set specially. Only according to transmission format of the 10 Bit Address to send the corresponding data.

18.5.5.2 10 Bit Address for I²C Slave

TEN_ADDR_EN=1 of I²C SOAUP (0x50003810), set ADDR[9:7] and ADDR[6:0]. And then, set DA=1, followed by the same as the original Slave program.

19. SPI Interface

19.1 FEATURES

- Full duplex Synchronous serial data transfer
- Configurable as a master or a slave on the interface
- Programmable clock bit rate (1/2 (master only), 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of MCU clock)
- Programmable data size from 4 bits to 16 bits
- Separate TXFIFO (8x16bits) and RXFIFO (8x16bits).
- Interrupts for TXFIFO and RXFIFO

19.2 PINS DESCRIPTION

PIN	GPIO	TYPE	DESCRIPTION
SPI_SCK	P0_03	INPUT / OUTPUT	SPI clock pin
SPI_MOSI	P0_02	INPUT / OUTPUT	Slave serial data input / Master serial data output
SPI_MISO	P0_01	INPUT / OUTPUT	Master serial data input / Slave serial data output
SPI_CS	P0_00	INPUT / OUTPUT	Slave select pin
SPI_SCK	P0_11	INPUT / OUTPUT	SPI clock pin
SPI_MOSI	P0_08	INPUT / OUTPUT	Slave serial data input / Master serial data output
SPI_MISO	P0_09	INPUT / OUTPUT	Master serial data input / Slave serial data output
SPI_CS	P0_10	INPUT / OUTPUT	Slave select pin

Table 19.1 SPI pins description

19.3 BLOCK DIAGRAM

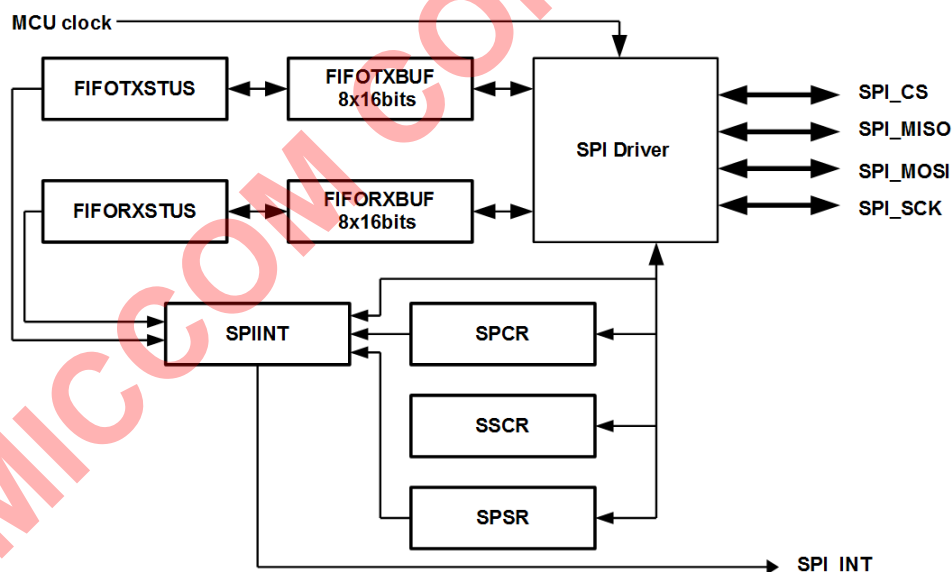


Figure 19.1 SPI Block Diagram

19.4 REGISTER

19.4.1 Register list

Address	Name	DESCRIPTION
0x50002000	SPCR	SPI Control Register
0x50002004	SPSR	SPI Status Register
0x50002008	SPIINT	SPI Interrupt Register
0x5000200C	SSCR	Slave Select Control Register
0x50002010	FIFOTXSTUS	SPI TX FIFO Status
0x50002014	FIFORXSTUS	SPI RX FIFO Status
0x50002018	FIFOTXBUF	SPI TX FIFO Buffer

0x5000201C	FIFORXBUF	SPI RX FIFO Buffer
0x50002400	SPCR	SPI Control Register
0x50002404	SPSR	SPI Status Register
0x50002408	SPIINT	SPI Interrupt Register
0x5000240C	SSCR	Slave Select Control Register
0x50002410	FIFOTXSTUS	SPI TX FIFO Status
0x50002414	FIFORXSTUS	SPI RX FIFO Status
0x50002418	FIFOTXBUF	SPI TX FIFO Buffer
0x5000241C	FIFORXBUF	SPI RX FIFO Buffer

Table 19.2 SPI register list

19.4.2 Register Description

SPCR (SPI Control Register)

Address: 0x50002000/0x50002400

R/W	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
W								
R	--							
Reset	0	0	0	0	0	0	0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W								
R	--	RXFIFO_IL[2:0]			--	TXFIFO_IL[2:0]		
Reset	0	0	1	1	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	SLAVE_RST			FIFOEN	BIT_LEN[3:0]			
R	--	--	--					
Reset	0	0	0	0	0	0	0	0
R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--	SPE	SPR[2]	MSTR	CPOL	CPHA	SPR[1]	SPR[0]
R	--							
Reset	0	0	0	0	0	1	0	0

RXFIFO_IL[2:0]: Set SPI RX FIFO interrupt level. If RXFIFO_IL[2:0] < RXFIFO_REM[2:0], generate interrupt.

TXFIFO_IL[2:0]: Set SPI TX FIFO interrupt level. If TXFIFO_IL[2:0] > TXFIFO_REM[2:0], generate interrupt

SLAVE_RST: In SPI Slave, write 1 to reset SPI TX FIFO point:

[0]: No effect

[1]: Reset SPI TX FIFO WP (only for SPI Slave)

FIFOEN: SPI FIFO mode enable

[0]: NOT SUPPORT

[1]: FIFO mode

BIT_LEN[3:0]: Set number of bits in a shift sequence:

[0~3]: 4 bits data

[4~15]: (BIT_LEN[3:0] + 1) bits data

SPE: SPI Enable

[0]: SPI disable

[1]: SPI enable

MSTR: SPI Master/ SPI Slave select

[0]: SPI Slave

[1]: SPI Master

CPOL: Clock polarity select

[0]: SPI_SCK idle low

[1]: SPI_SCK idle high

CPHA: Clock phase select

[0]: Latch data in first SPI_SCK edge change

[1]: Latch data in second SPI_SCK edge change

SPR[2:0]: SPI clock rate select bits:

SPR2	SPR1	SPR0	MCU clock divided by
0	0	0	4
0	0	1	8
0	1	0	16
0	1	1	32
1	0	0	64
1	0	1	128
1	1	0	256
1	1	1	2 (only for SPI Master)

SPSR (SPI Status Register)

Address: 0x50002004/0x50002404

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--		--	--				SSCEN
R			SS_S					
Reset	0	0	0	0	0	1	0	0

SS_S: In SPI Salve, this bit connected with SPI_CS.

SSCEN: SPI_CS automatic select setting. This bit work with SS0.

SSCEN	SS0	SPI_CS
0	0	0
0	1	1
1	0	0 when transfer. 1 when idle.
1	1	1

SPIINT (SPI Interrupt Register)

Address: 0x50002008/0x50002408

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--		RXFIFO_INT_FLAG	TXFIFO_INT_FLAG	--		RXFIFO_INTEN	TXFIFO_INTEN
R								
Reset	0	0	0	0	0	0	0	0

RXFIFO_INT_FLAG: RXFIFO interrupt flag

[0]: Interrupt not occurs.

[1]: Interrupt occurred, write 1 to clear.

TXFIFO_INT_FLAG: TXFIFO interrupt flag

[0]: Interrupt not occurs.

[1]: Interrupt occurred, write 1 to clear.

RXFIFO_INTEN: SPI RXFIFO interrupt enable

[0]: Disable

[1]: Enable

TXFIFO_INTEN: SPI TXFIFO interrupt enable

[0]: Disable

[1]: Enable

NOTE: User need clear RXFIFO_INT_FLAG and TXFIFO_INT_FLAG before write FIFOTXBUF when SPI interrupt occur.

SSCR (SPI Select Control Register)

Address: 0x5000200C/0x5000240C

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-----	-------	-------	-------	-------	-------	-------	-------	-------

W	--							SS0
R								
Reset	1	1	1	1	1	1	1	1

SS0: SPI_CS select. This bit work with SSCEN.

SSCEN	SS0	SPI_CS
0	0	0
0	1	1
1	0	0 when transfer. 1 when idle.
1	1	1

FIFOTXSTUS (FIFO TX Status)

Address: 0x50002010/0x50002410

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--			--	--	--		
R	--			TX_FULL	TX_EMPTY	TXFIFO_REM[2:0]		
Reset	0	0	0	0	1	0	0	0

TX_FULL: FIFOTXBUF Full

[0]: FIFOTXBUF not full, user can write data to FIFOTXBUF.

[1]: FIFOTXBUF full, user can't write data to FIFOTXBUF.

TX_EMPTY: FIFOTXBUF Empty

[0]: FIFOTXBUF not empty.

[1]: FIFOTXBUF empty.

TXFIFO_REM [2:0]: FIFOTXBUF remnant. The number of data in the FIFOTXBUF

TX_FULL	TX_EMPTY	TXFIFO_REM[2:0]	Number of data in FIFOTXBUF
0	1	0	0
0	0	0	1
0	0	1	2
0	0	2	3
0	0	3	4
0	0	4	5
0	0	5	6
0	0	6	7
1	0	7	8

FIFORXSTUS (FIFO RX Status)

Address: 0x50002014/0x50002414

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--			--	--	--		
R	--			RX_FULL	RX_EMPTY	RXFIFO_REM[2:0]		
Reset	0	0	0	0	1	0	0	0

RX_FULL: FIFORXBUF Full

[0]: FIFORXBUF not full.

[1]: FIFORXBUF full.

RX_EMPTY: FIFORXBUF Empty

[0]: FIFORXBUF not empty.

[1]: FIFORXBUF empty. Read FIFORXBUF will read as 0.

RXFIFO_REM [2:0]: The numbers of data in the FIFORXBUF

RX_FULL	RX_EMPTY	RXFIFO_REM[2:0]	Numbers of data in FIFORXBUF
0	1	0	0
0	0	1	1
0	0	2	2
0	0	3	3
0	0	4	4
0	0	5	5
0	0	6	6
0	0	7	7
1	0	0	8

FIFOTXBUF (FIFO TX Buffer)

Address: 0x50002018/0x50002418

R/W	Bit 15	-----	Bit 0
W	TXBUF[15:0]		
R	--		
Reset	0x0000		

TXBUF[15:0]: FIFOTXBUF is a FIFO register with a width of 16 bits and depth of 8. User can write data to this FIFO and send out via SPI. Refer to 19.5.4 SPI FIFO for details.

FIFORXBUF (FIFO RX Buffer)

Address: 0x5000201C/0x5000241C

R/W	Bit 15	-----	Bit 0
W	--		
R	RXBUF[15:0]		
Reset	0x0000		

RXBUF[15:0]: FIFORXBUF is a FIFO register with a width of 16 bits and depth of 8. Data will be saved to FIFORXBUF when SPI received data. User can read out data from FIFORXBUF. Refer to 19.5.4 SPI FIFO for details.

19.5 FUNCTION DESCRIPTION

19.5.1 SPI Master and SPI Slave

SPI Driver can be set to SPI Master (MSTR=1) or SPI Slave (MSTR=0) via MSTR. When SPI Driver is set to SPI Master, SPI_CS and SPI_SCK will be controlled by SPI Driver, and send data via SPI_MOSI, receive data via SPI_MISO. When SPI Driver is set to SPI Slave, SPI_CS and SPI_SCK will be controlled by other SPI, and receive data via SPI_MOSI, send data via SPI_MISO.

19.5.2 SPI_SCK speed

Speed of SPI is decides by speed of SPI_CLK. Speed of SPI_CLK is related to MCU Clock. Speed can be adjusted by SPR2, SPR1 and SPR0:

SPR2	SPR1	SPR0	MCU clock divided by
0	0	0	4
0	0	1	8
0	1	0	16
0	1	1	32
1	0	0	64
1	0	1	128
1	1	0	256
1	1	1	2 (only for SPI Master)

Table 19.3 SPI pins description

For example:

System Clock is 16MHz and SPR2=0, SPR1=0, SPR0=0, speed of SPI_CLK is 4MHz (16MHz / 4). Therefore, speed of SPI is 4M bps.

It needs to be noted, the set SPR2=1, SPR1=1, SPR0=1 is only for SPI Master, SPI Slave does not use this set.

19.5.3 SPI Transmission Format

19.5.3.1 SPI Transmission Data Length

SPI can set every transmission data length via BIT_LEN[3:0] of SPCR. Data length can be set during 4~16 Bits.

For example:

Each data of SPI will transmit 4 bits when BIT_LEN[3:0]=3.

Each data of SPI will transmit 16 bits when BIT_LEN[3:0]=15.

19.5.3.2 SPI_CS Setting

In SPI Master, SPI_CS can be set auto selection mode or manual selection mode. Description is as follows:

Auto selection mode: When SSCEN=1, SS0=0, SPI_CS will be pulled low automatically at data is transmitting and SPI_CS will be pulled high automatically at data transmitting is complete. Shown is as following figure:

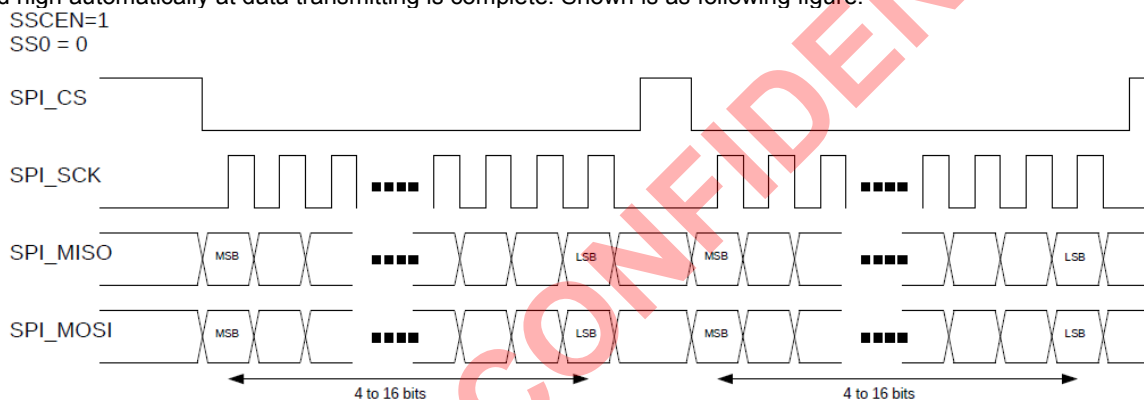


Figure 19.2 SPI_CS auto selection mode

Manual selection mode: When SSCEN=0, SPI_CS is controlled by SS0, SPI_CS will be pulled low when SS0=0; SPI_CS will be pulled high when SS0=1. Shown is as following figure:

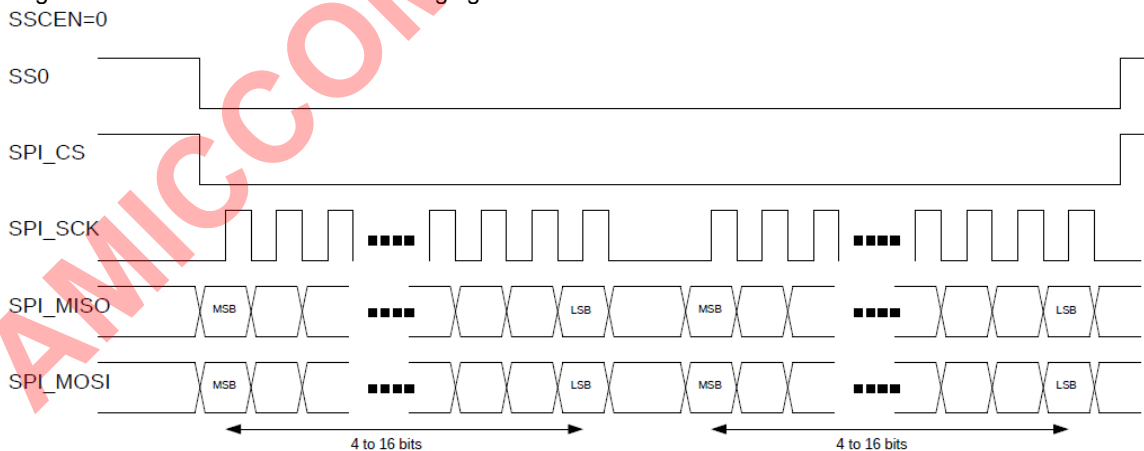


Figure 19.3 SPI_CS manual selection mode

19.5.3.3 SPI_SCK Setting

SPI can support four kinds of transmission format via CPOL and CPHA of SPCR. SPI_SCK is set by CPOL at idle state. When CPOL=0, SPI_SCK is low at idle state. When CPOL=1, SPI_SCK is high at idle state. CPHA is used to set which number of SPI_SCK to occur changed and start to latch data. When CPHA=0, start to latch data at SPI_SCK occurs changed first time. When CPHA=1, start to latch data at SPI_SCK occurs changed second time.

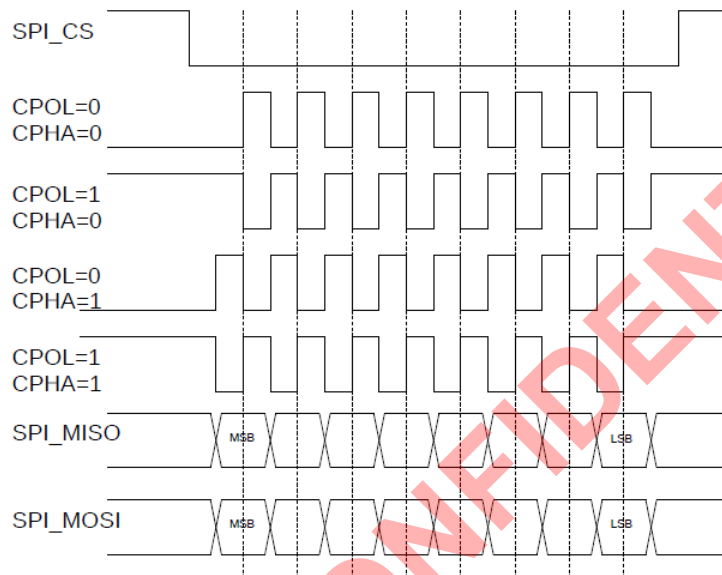


Figure 19.4 The dotted line represents timing to latch data.

19.5.4 SPI FIFO

The SPI has two separate FIFO, one is SPI TX FIFO, and the other is SPI RX FIFO. These two FIFO are with a width of 16 bits and depth of 8. They can be used to send/receive data continuously.

WP (write point) will move up when data is written to FIFOTXBUF.

WP (write point) will move down when data of SPI Master's MOSI or data of SPI Slave's MISO is sent out.

RP (read point) will move up when data of SPI Master's MISO or data of SPI Slave's MOSI is received.

RP (read point) will move down when data is read.

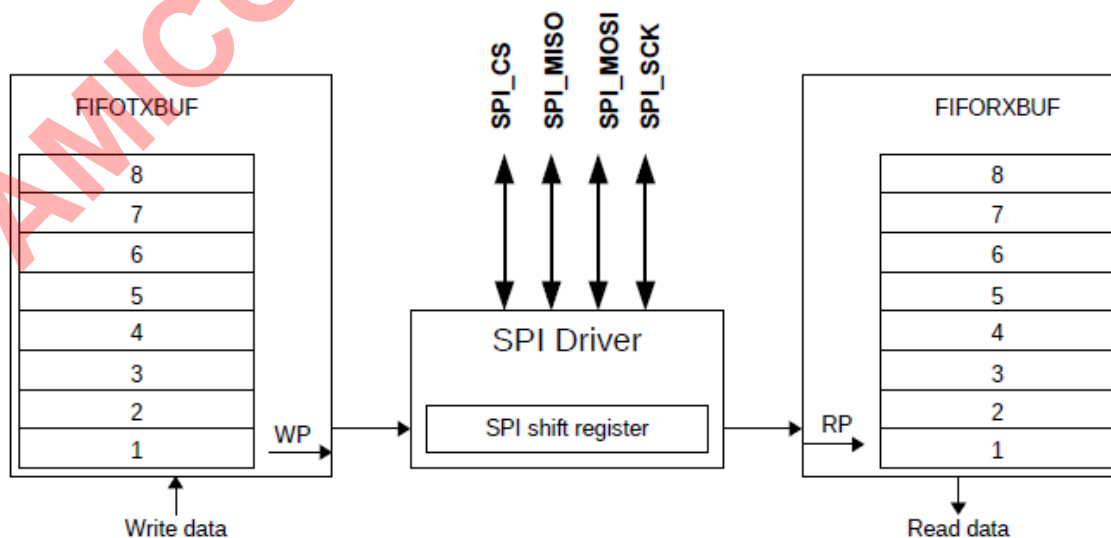


Figure 19.5 SPI FIFO Architecture descriptions

19.5.5 SPI FIFO interrupt

SPI FIFO interrupt, it must be $RXFIFO_INTEN=1$ of SPIINT or $TXFIFO_INTEN=1$ of SPIINT, and $SPI_INT=1$ of NVIC. Please refer to Table 11.2 Interrupt Map Vector Table.

And then, when data number of SPI TX FIFO or data number of SPI RX FIFO reaches to set value of $TXFIFO_IL[2:0]$ or $RXFIFO_IL[2:0]$. SPI interrupt will be started. User can read $TXFIFO_INT_FLAG$ and $RXFIFO_INT_FLAG$ to determine the interruption is generated by SPI TX FIFO or SPI RX FIFO.

Please be noted, $TXFIFO_INT_FLAG$ and $RXFIFO_INT_FLAG$ should be cleared to zero by user. And then, $FIFOTXBUF$ can be written data or read data from $FIFORXBUF$.

SPI TX FIFO interrupt condition: $TXFIFO_IL[2:0] > TXFIFO_REM[2:0]$
 SPI RX FIFO interrupt condition: $RXFIFO_IL[2:0] < RXFIFO_REM[2:0]$

Please refer to 19.5.6.1 SPI Master Transmit data and 19.5.6.2 SPI Master Receive data

19.5.6 SPI Master Transmit

When SPI Driver is set to SPI Master, data can be written from $FIFOTXBUF$ to SPI TX FIFO and data can be read from SPI RX FIFO via $FIFORXBUF$. At the same time, state of SPI TX FIFO and SPI RX FIFO can be checked by $FIFOTXSTUS$ and $FIFORXSTUS$, and write/read data at the right time to keep writing/reading data continuously.

19.5.6.1 SPI Master Transmit data

When $TX_FULL=0$, data can be written to $FIFOTXBUF$ by user. When $TX_FULL=1$, data can't be written to SPI TX FIFO if user keeps writing data continuously. When there is data in SPI TX FIFO, data will be sent by SPI_MOSI at SPI Master. At the same time, data will be read by SPI_MISO and will be saved to SPI RX FIFO.

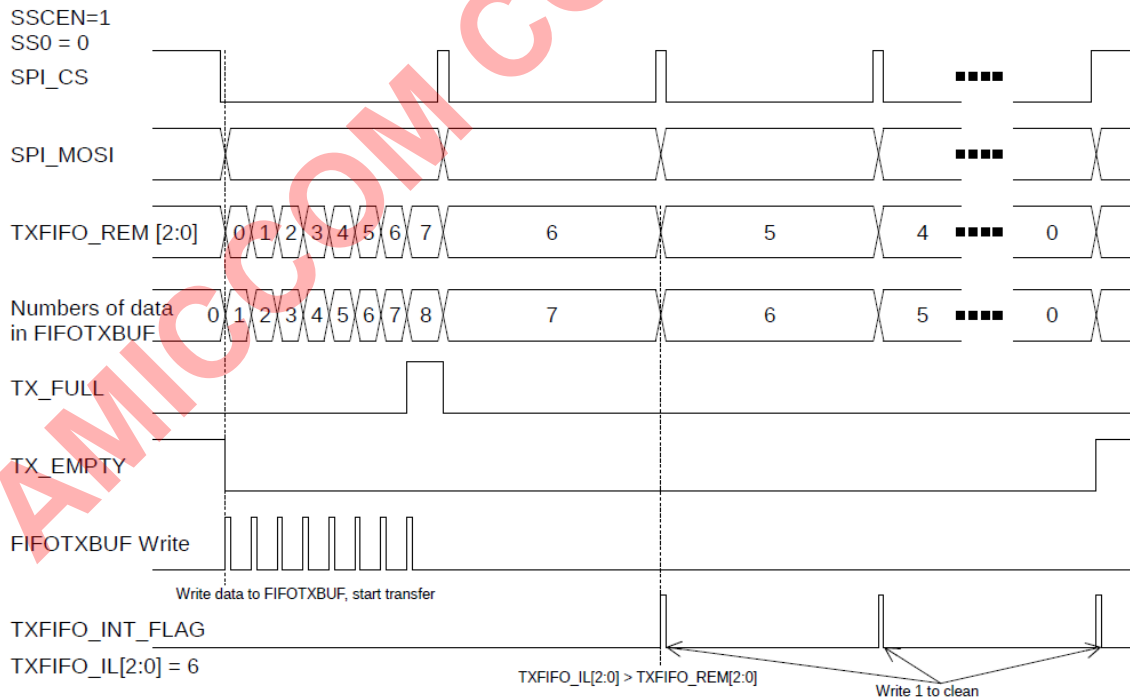


Figure 19.6 An example for SPI Master sent data 8 times and set $TXFIFO_IL[2:0]=6$

19.5.6.2 SPI Master Receive data

When SPI Master is sending data, SPI will receive data and save to SPI RX FIFO at the same time. When RX_FULL=1, data will be not written to SPI RX FIFO.

SSCEN=1

SS0 = 0

SPI_CS

SPI_MISO

RXFIFO_REM [2:0]

Numbers of data
in FIFORXBUF

RX_FULL

RX_EMPTY

FIFORXBUF Read

RXFIFO_INT_FLAG

RXFIFO_IL[2:0] = 1

RXFIFO_IL[2:0] ← RXFIFO_REM[2:0]

Write 1 to clean

Figure 19.7 An example SPI Master received data 8 times and set RXFIFO_IL[2:0]=1

Please refer the "SampleCode\A8125M0\SPI_Master" for setup SPI master and SPI master interrupt.

Please refer the "SampleCode\A8125M0\SPI_Slave" for setup SPI slave and SPI slave interrupt.



19.5.7.1 SPI Slave Transmit data

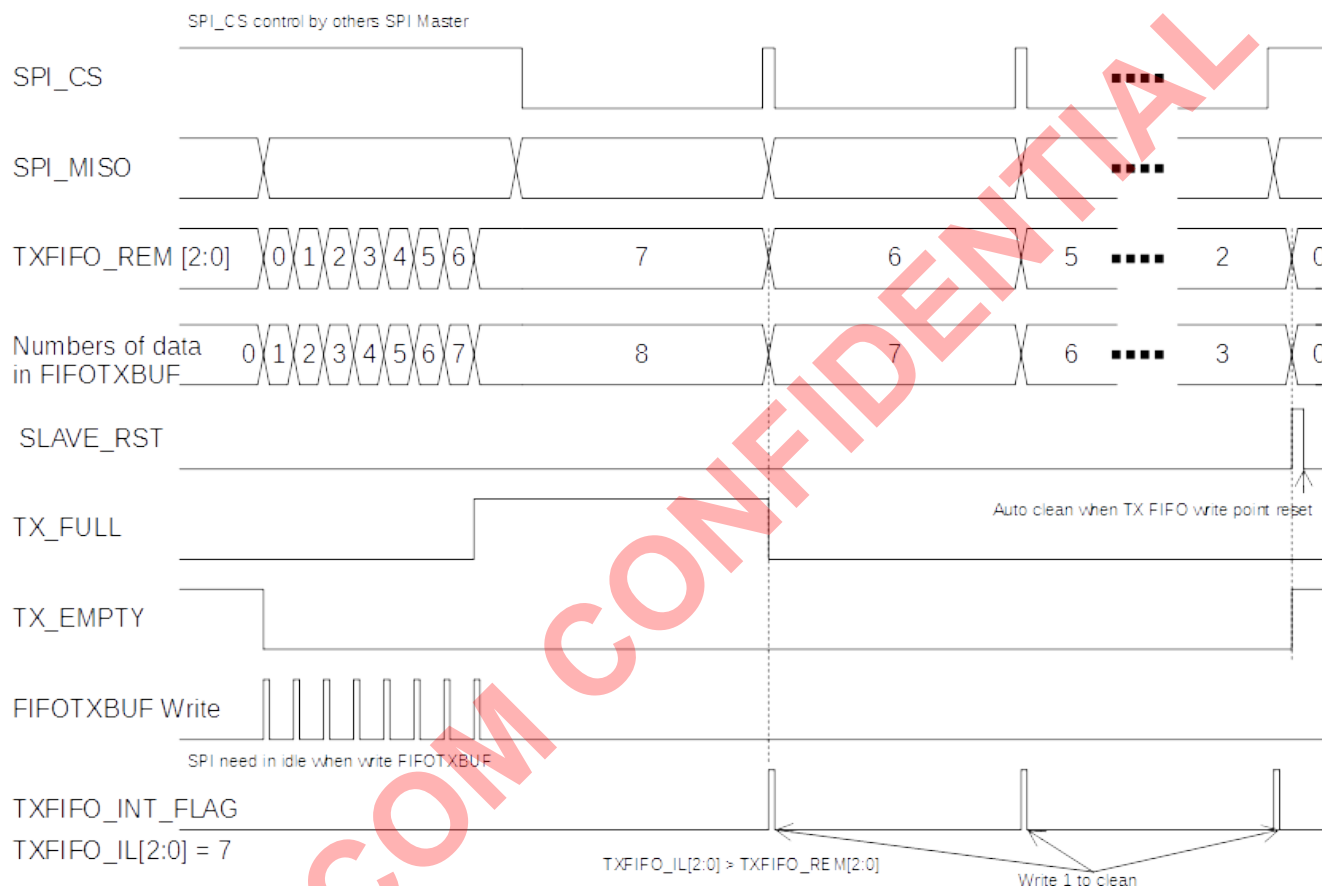


Figure 19.8 An example for SPI Slave wrote data 8 times in advance, and sent out data when received data.

19.5.7.2 SPI Slave Receive data

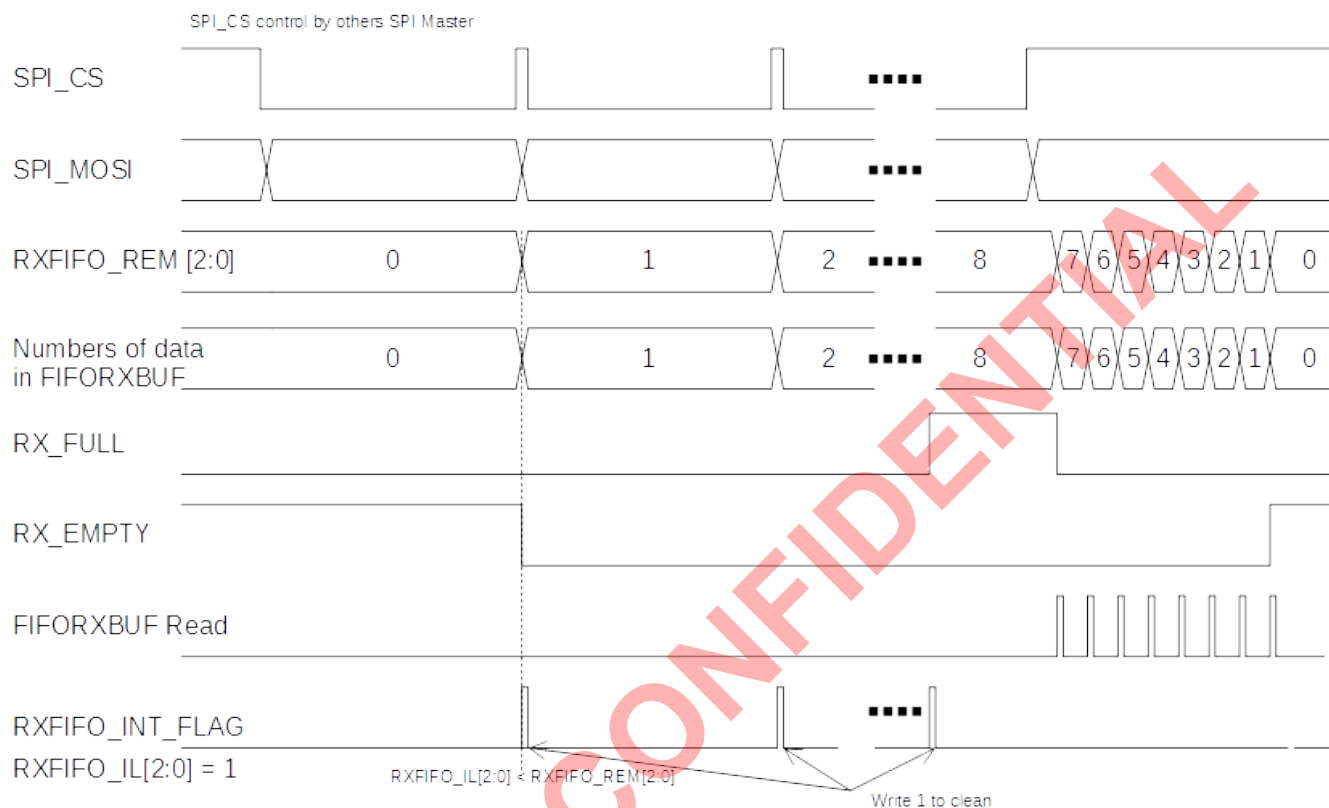


Figure 19.9 An example for SPI Slave received data 8 times

20. Power Management

A8125M0 has four power management modes: Normal mode and PMx mode. In normal mode, user selects different clock being MCU core clock.in CLKSEL[2:0] then enable CKSE. User adjusts MCU clocks depending on the required power consumption.

PM mode includes PM1, PM2 and PM3. User can set STOP=1 into PMx mode, so that the clock to the core is stopped and all digital peripherals also stop. MCU can be waked up by hardware reset, wakeup key, sleep timer and RTC.

Note: Please don't enable STOP and CKSE at the same time.

	MCU speed	XOSC	SRAM	LVD	RF	Back to Normal (Wakeup)
Normal CKSE=0	F _{XTAL}	ON	ON	X	X	
Normal CKSE=1 (Low speed)	F _{XTAL} /2/4/8/16, IRC/RTC	ON	ON	X	X	
PM1	STOP	OFF	ON	X	OFF	Reset pin/WUN/Sleep timer
PM2	STOP	OFF	ON	X	OFF	Reset pin/WUN/Sleep timer
PM3	STOP	OFF	1KB retention	X	OFF	Reset pin/WUN/Sleep timer
Deep sleep	STOP	OFF	OFF	OFF	OFF	Reset pin/WUNIE

X: don't care, it can turn on or off by user setting
LVD: Low Voltage Detect
WUN: Wakeup pin, setting by WUN
WUNIE: Only P0.14, P0.15, P0.16, P0.17(This function will be auto active in deep sleep mode)
Note:
1. In PM1 and PM2 user can select SRAM size for 1kB, 4kB or 32kB (see Figure 20.2).
2. PM3 and deep sleep need to initial peripheral after wake up.

Table 20.1 Power management

20.1 BLOCK DIAGRM

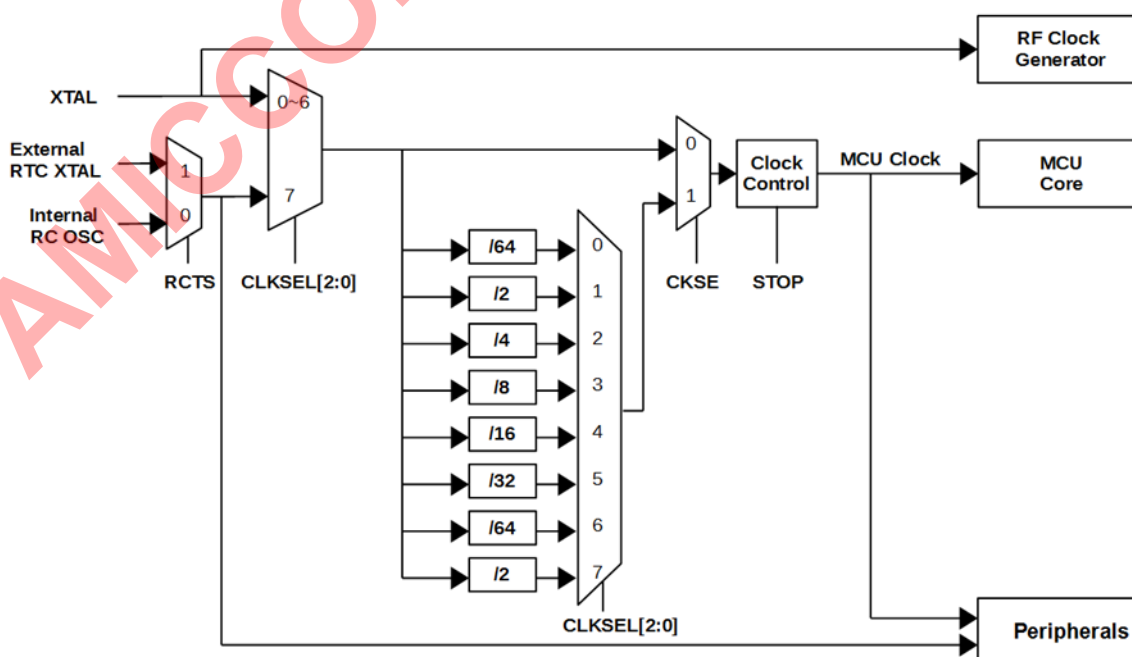


Figure 20.1 Whole chip clock sources

20.2 REGISTER

20.2.1 Register List

Address	Name	DESCRIPTION
0x50000008	Power Control I	Power Control I Register

Table 20.2 Power Management Register List

20.2.2 Register Description

Power Control I Register (Address: 0x50000008)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PDNDS	PMVSDS	PWMS	PM1S	QD	REGAE	PM3S	STOP
R	--	--	--	--	--	--	--	--
Reset	0	1		0	0	0	0	0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	PM1SW1	PM1SW0	CPPSN	PMPAR	CLKSEL2	CLKSEL1	CLKSEL0	PMM
R	--	--	--	--	--	--	--	--
Reset	0	0	1	1	0	0	0	0

PM1S(Power Mode 1 select)

[0]: Deselect

[1]: Select

QD(Quick discharge Enable)

[0]: Disable

[1]: Enable

PM3S (Power Mode 3 select)

[0]: Deselect

[1]: Select

STOP (Stop mode)

[0]: Disable

[1]: Enable

CLKSEL[2:0] (Clock Select), Select clock source when enable clock select.

[000]: Clock source div 64 as MCU clock

[001]: Clock source div 2 as MCU clock

[010]: Clock source div 4 as MCU clock

[011]: Clock source div 8 as MCU clock

[100]: Clock source div 16 as MCU clock

[101]: Clock source div 32 as MCU clock

[110]: Clock source div 64 as MCU clock

[111]: Select RTC as CPU clock when CKSE=0; RTC div 2 as CPU clock when CKSE=1

20.3 FUNCTION DESCRIPTION

20.3.1 Normal Mode

In normal mode, user selects different clock be MCU core clock.in CLKSEL[2:0] then enable CKSE .User adjusts MCU clocks depending on the required power consumption. CLKSEL[2:0] = 001b ~ 110b, the MCU core clock is the clock sources divided 2 ~ 64. User could adjust the MCU speed to trade-off between the performance and the power consumption.

To perform Normal mode, follow these steps:

1. CKSE = 0
2. Set CLKSEL[2:0] to select clock source
3. CKSE = 1

20.3.2 PM Mode

User can STOP MCU clock and some circuit, peripherals to save current consumption:

PM Mode	Power Control I 0x50000008	Digital Power	Analog Power
PM1	PM1S = 1, STOP = 1	ON	ON
PM2	QD = 1, STOP = 1	ON	OFF
PM3	PM3S = 1, STOP = 1	OFF	OFF
Deep sleep	MT[2:0] = 0, STOP = 1	OFF	OFF

Table 20.3 Power control register I setting for PM Mode

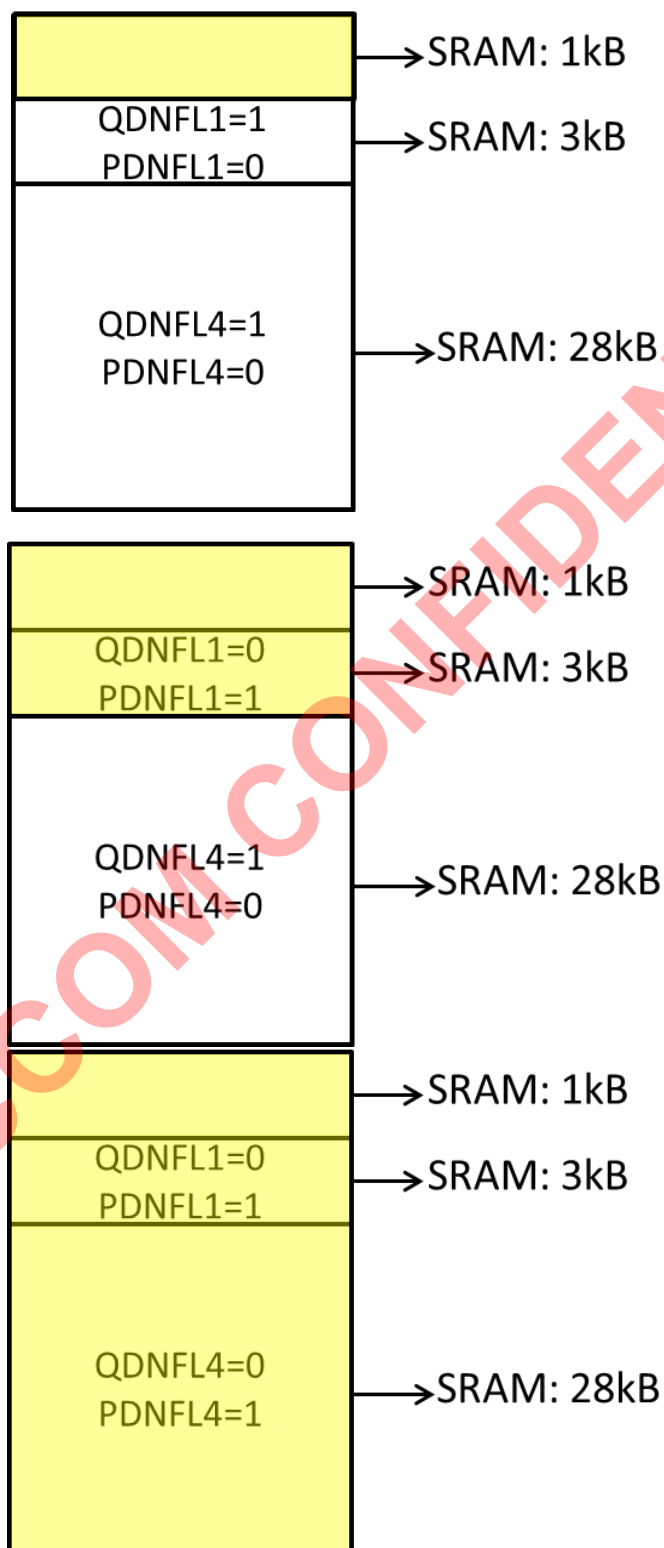
To perform PMx, follow these steps:

1. If CKSE = 1, set it to 0
2. Set Power Control I (0x50000008) value by PMx mode.
3. Set Flash Control (0x50000004) = 0x00001595
4. STOP = 1 to enter PMx mode

Deep sleep set up steps:

1. Set IO mode control (0x50000024) = 0x00010000 for deep sleep.
2. STOP = 1 to enter deep sleep mode.

SRAM size setting:



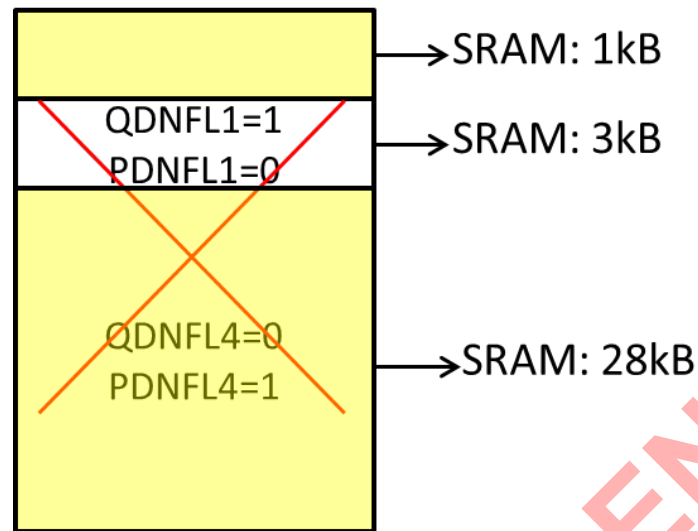


Figure 20.2 SRAM size

21. 8-bits ADC

A8125M0 has built-in 8-bits ADC (Analog to Digital Converter). The 8-bits ADC can be used to measure the carrier detect and RSSI.

21.1 FEATURES

- For carrier detect, RSSI measurement.

21.2 BLOCK DIAGRM

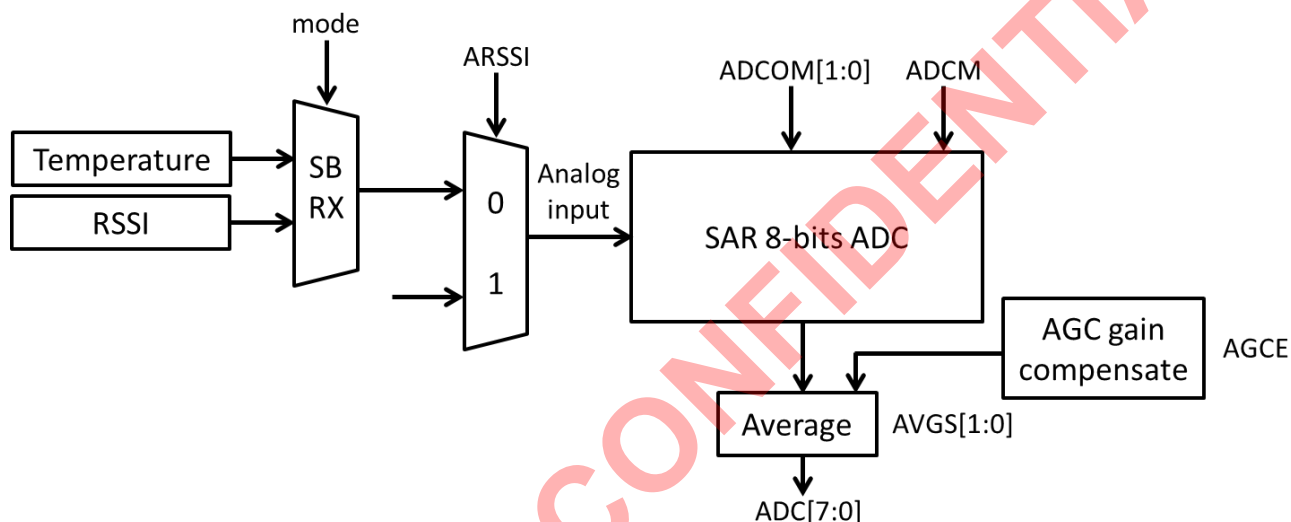


Figure 21.1 8-bits ADC block diagram

21.3 REGISTER

21.3.1 Register List

Address	Name	DESCRIPTION
0x50001240	ADC Control	ADC Control Register
0x50001244	ADC Threshold	ADC Threshold Register / ADC value

Table 21.1 8-bits ADC register list

21.3.2 Register Description

8BIT ADC Control Register (Address: 0x50001240)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	ADCC	ADCOM[1:0]	AVGS[1:0]	ARSSI	CDM	ADCM		
R								
Reset	0	1	0	1	1	1	1	0

ADCOM: ADC output mode.

[00]: Single mode.

[01]: ED average mode (2, 4, 8, 16 average is according to AVGS [1:0].

[10]: Reserved.

[11]: ED. Hold after sync 128us.

AVGS [1:0]: ADC average mode.

[00]: 2.

[01]: 4.

[10]: 8.
[11]: 16.

ARSSI: Auto RSSI measurement whenever in RX mode..

[0]: Disable.
[1]: Enable.

CDM: CD margin = CDTH – CDTL.

[0]: 6 LSB.
[1]: 12 LSB.

ADCM: ADC measurement (Auto clear when done).

[0]: Disable.
[1]: Enable.

8Bit ADC Threshold Register (Address: 0x50001244)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CDTH[7:0]							
R	ADC[7:0]							
Reset	0	1	1	0	0	1	0	0

CDTH [7:0]: Carrier detect threshold.

ADC [7:0]: ADC digital output value.

ADC input voltage = 0.6 * ADC [7:0] / 256 V.

21.4 FUNCTION DESCRIPTION

21.4.1 8-bits ADC function:

The 8-bits ADC provides RSSI and carrier detect measurement.

ADCM	MODE	
	Standby	RX
[0]	None	None
[1]	Measure temperature or external voltage	RSSI / Carrier detect

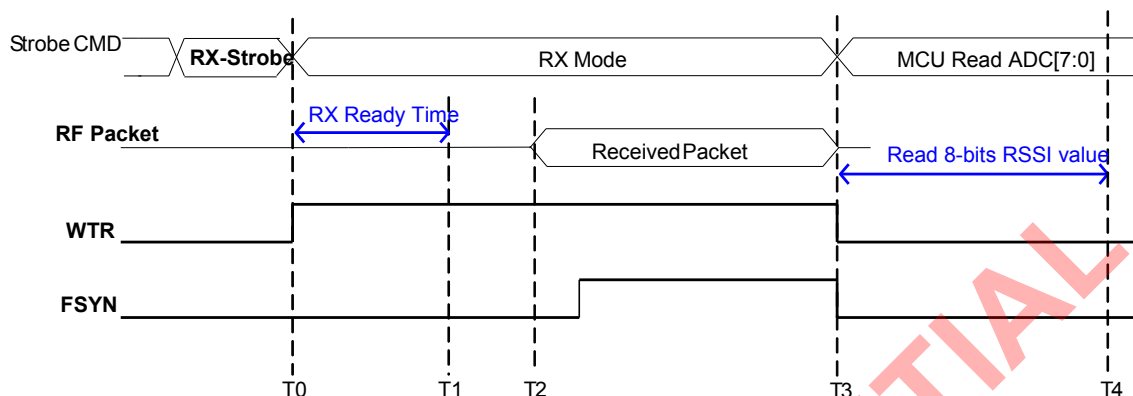
Table 21.2 8-bits ADC setting

21.4.2 RSSI measurement:

A8125M0 supports 8-bits digital RSSI to detect RF signal strength. RSSI value is stored in ADC [7:0](0x50001244). A8125M0 automatically averages 2/4/8/16-times for RSSI measurement until A8125M0 exits RX mode. Therefore, maximum RSSI measuring time is $(16 \times 20 / F_{ADC})$. Be aware RSSI accuracy is about $\pm 6\text{dB}$.

Auto RSSI measurement for TX Power:

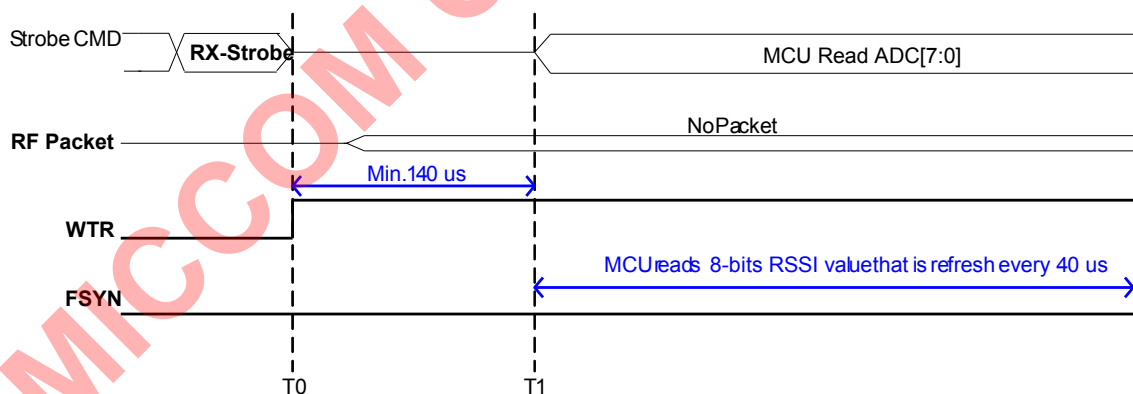
1. Set VDD_AD(PAV) = 1.2V (0x50001104)
2. Set wanted channel.(0x500010C0)
3. Set ADC out mode: ED no hold, average mode: 16, Enable ARSSI = 1. (0x50001240)
4. Send RX strobe command.
5. In RX mode, average RSSI measurement periodically.
6. When RX synchronize finished. User can read RSSI value from ADC [7:0] (0x50001244) for TX power.



T0-T1: Settling Time
T2-T3: Receiving Packet
T3 : Exit RX mode automatically in FIFO mode
T3-T4 MCU read RSSI value @ ADC [7:0]
Figure 21.2 RSSI Measurement of TX Power.

Auto RSSI measurement for Background Power:

1. Set VDD_AD(PAV) = 1.2V (0x50001104)
2. Set wanted channel.(0x500010C0)
3. Set ADC out mode: ED no hold, average mode: 16, Enable ARSSI = 1. (0x50001240)
4. Send RX Strobe command.
5. MCU delays min. 140us.
6. Read digital RSSI value from ADC [7:0] (0x50001244) to get background power.
7. Send other Strobe command to let A8125M0 exit RX mode.



T0-T1: MCU Delay Loop from PLL to RX mode for RSSI measurement
T1 : Auto RSSI Measurement is done by 8-times average.
MCU can read RSSI value from ADC [7:0]

Figure 21.3 RSSI Measurement of Background Power.

21.4.3 Carrier Detect

Base on RSSI measurement, user can extend its application to do carrier detect (CD). In Carrier Detect mode, RSSI is refresh every 5 us without 8-times average. If RSSI level is above threshold level (CDTH), CD is output high to GIO1 or GIO2 pin to inform MCU that current channel is busy.

Below is a reference procedure:

1. Set CDTH for absolute RSSI threshold level.

2. Set GIO2S = [0010] for Carrier Detect to GIO2 pin.
 - (2-1) Set wanted F_{RXLO} .
 - (2-2) Set CDM (CDM =0 and hysteresis =6, or CDM =1 and hysteresis =12).
 - (2-3) Enable ARSSI= 1.
 - (2-4) Send RX Strobe command.
 - (2-5) MCU enables a timer delay (min. 100 us).
3. MCU checks GIO2 pin.
 - (3-1) If $ADC \geq CDTH$, GIO2 = 1.
 - (3-2) If $ADC \leq CDTH-CDM$, GIO2 = 0.
 - (3-3) If ADC locates in hysteresis zone, GIO2 = previous state.
4. Exit RX mode.

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22. 12-bits SAR ADC

A8125M0 includes a 12-bits successive approximation A/D converter which enables channel selection from 8 channels. The A/D converter has two operating modes: single mode and continuous mode. The 12-bits A/D converter can be used to perform the analog input of the specified channel.

22.1 FEATURE

- External Voltage measure from 8 channels.
- Programmable internal reference voltage.
- Application measuring for sensor interface, battery operated system, data acquisition.

22.2 PINS DESCRIPTION

PIN	GPIO	TYPE	DESCRIPTION
ADCIO0	P0_18	INPUT	12-bits ADC analog input channel 0
ADCIO1	P0_19	INPUT	12-bits ADC analog input channel 1
ADCIO2	P0_08	INPUT	12-bits ADC analog input channel 2
ADCIO3	P0_09	INPUT	12-bits ADC analog input channel 3
ADCIO4	P0_12	INPUT	12-bits ADC analog input channel 4
ADCIO5	P0_13	INPUT	12-bits ADC analog input channel 5
ADCIO6	P0_14	INPUT	12-bits ADC analog input channel 6
ADCIO7	P0_15	INPUT	12-bits ADC analog input channel 7

Table 22.1 12-bits ADC pins description

22.3 BLOCK DIAGRM

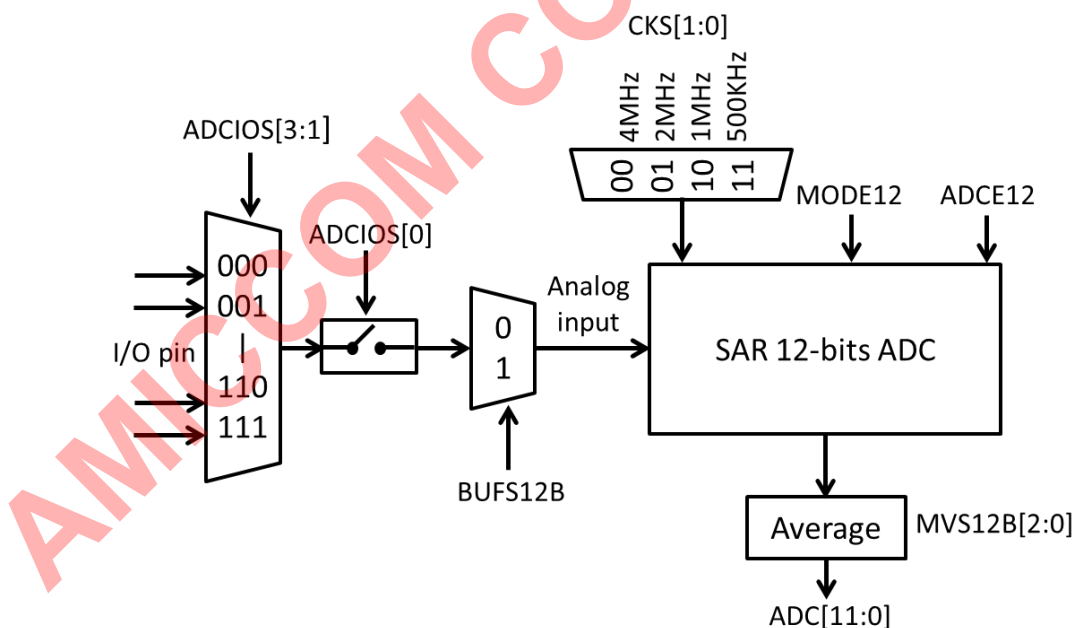


Figure 22.1 12-bits ADC block diagram

22.4 REGISTER

22.4.1 Register List

Address	Name	DESCRIPTION
0x50008000	ADC Control	12-bits ADC Control Register
0x50008004	ADC Value	12-bits ADC Value Register
0x50008008	ADC INT_State	12-bits ADC INT_State Register

Table 22.2 12-bits ADC register list

22.4.2 Register Description

12bit ADC Control Register (Address: 0x50008000)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	BUFS12B	--		MODE12	MVS12[2:0]			ADCE12
R	--			MODE12				ADCE12
Reset	0			0	0x0			0
R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	ADCIOS[3:1]			ADCIOS[0]	--		ADIVL	ADCYC
R	--			--			--	--
Reset	0x0			0			0	0
R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
W	--				CKS[1:0]		DELS[1:0]	
R					--		--	
Reset	0x0				0	0	0	0

BUFS12B: buffer select for 12bit ADC.

[0]: disable

[1]: enable

MODE12: ADC 12bit mode.

[0]: single mode.

[1]: continuous.

MVS12B [2:0]: 12bit ADC moving average mode.

[000]: no average

[001]: average 2 times

[010]: average 4 times

[011]: average 8 times

[100]: average 16 times

[101]: average 32 times

[110]: average 64 times

[111]: average 128 times

ADCE12: ADC 12bit measurement enable.

[0]: disable

[1]: enable.

ADCIOS[0]: ADC I/O enable

ADCIOS[3:1]: ADC I/O select.

[000]: P0_18

[001]: P0_19

[002]: P0_08

[003]: P0_09

[004]: P0_12

[005]: P0_13

[006]: P0_14

[007]: P0_15

ADIVL: ADC 12bit initial value.

[0]: 0
[1]: 2048

ADCYC: ADC 12bit counter reference.

[0]: 31
[1]: 32

CKS[1:0]: ADC 12bit main clock select.

[00]: 4M
[01]: 2M
[10]: 1M
[11]: 0.5M

DELS[1:0]: ADC 12bit measurement delay select.

[00]: 5us
[01]: 10us
[10]: 15us
[11]: 20us

12bit ADC Register (Address: 0x50008004)

R/W	Bit 31	-----	Bit 12	Bit 11	-----	Bit 0
W	---					
R	---			ADC[11:0]		
Reset						

ADC12 [11:0]: ADC 12bit value.

12bit ADC INTSTATE Register (Address: 0x50008008)

R/W	Bit 31	-----	Bit 1	Bit 0
W	---			ADCI_Clear
R	---			ADCI_STATE
Reset				0

ADCI_Clear: ADC 12bit INT clear.

[0]: normal
[1]: clear

ADCI_STATE: ADC 12bit INT State.

22.5 FUNCTION DESCRIPTION

A8125M0 includes a 12-bit successive approximation A/D converter which enables channel selection from 8 channels. The A/D converter has two operating modes: single mode and continuous mode.

22.5.1 ADC Value Calculation:

12 Bit ADC can be used to measure the external input. The input voltage range is from 0V ~ VREF_AD. Please care the input voltage if set the input source from external input. Refer to the following formula, input voltage can be calculated from ADC[11:0].

$$\text{ADC input voltage} = \frac{VREF_AD \times ADC[11:0]}{4095}$$

22.5.2 A/D Conversion Time:

The time of A/D conversion 1 times is:

$$T_{conv} = \frac{4 \times 2^{CKS[1:0]}}{MCU \text{ clock frequency}} \times 32$$

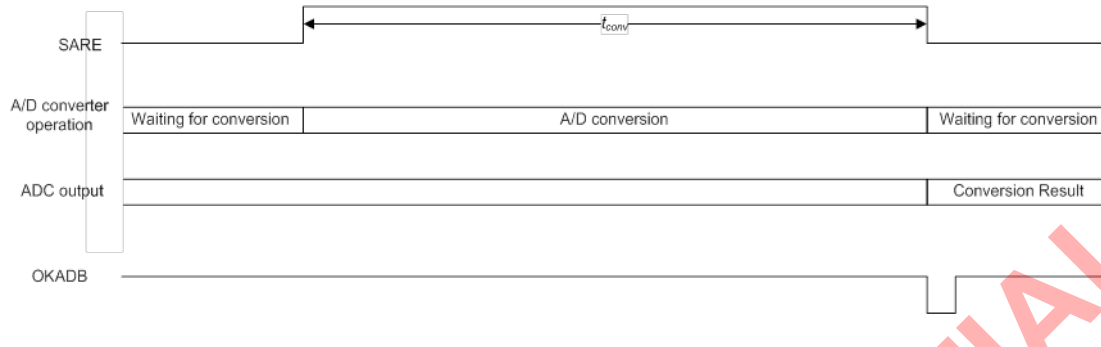


Figure 22.2 Single Mode for A/D Conversion.

22.5.3 Analog Input (Voltage) Measurement

Measurement for Analog Input:

1. Set DC-DC voltage(REG) = 2.0V (0x5000001C)
2. Set VDD_AD(PAV) = 1.8V (0x50001104)
3. Set ADCIOS(0x50008000) for selecting ADC channel.
4. Set MODE12=1(0x50008000) to select continuous mode and average mode (MVS12B).
5. Set ADCE12=1(0x50008000) to enable ADC.
6. Delay ADC conversion time.
7. Read ADC output from ADC12 [11:0](0x50008004).
8. Set ADCE12=0(0x50008000) to disable ADC.
9. Set back VDD_AD(PAV) = 1.2V (0x50001104)
10. Set back DC-DC voltage to 1.4V (0b5000001C)

23. Battery Detect

The Battery detect function can be used to detect a low battery condition with setting voltage threshold. This is useful for warning that regulation voltages could no longer be maintained. Then MCU has the time to provide hardware protection of data stored in the program memory.

23.1 FEATURE

- Programmable voltage detection threshold in 8 levels.

23.2 PIN DESCRIPTION

PIN	GPIO	TYPE	DESCRIPTION
VDD_IO	--	INPUT	VDD_IO supply voltage input

Table 23.1 Battery detect pin description

23.3 BLOCK DIAGRAM

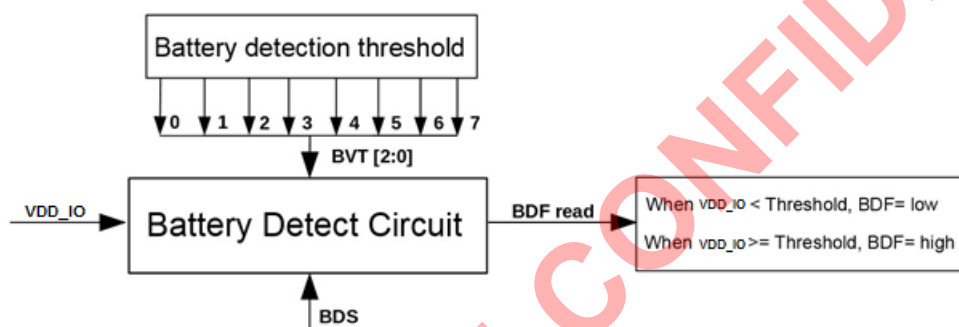


Figure 23.1 Battery detect Block Diagram

23.4 REGISTER

23.4.1 Register List

Address	Name	DESCRIPTION
0x50000000	Battery detect	Battery detect Register

Table 23.2 Battery detect register list

23.4.2 Register Description

Battery detect Register (Address: 0x50000000)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	---			BLE	BDV[2:0]			BDE
R								BDF
Reset				0	0	0	1	0

BLE: Battery life extension. Reserved for internal usage.

BDV[2:0]: Battery detection voltage.

[000]: 2.0V.

[001]: 2.1V.

[010]: 2.2V.

[011]: 2.3V.

[100]: 2.4V.

[101]: 2.5V.

[110]: 2.6V.

[111]: 2.7V.

BDE: Battery detection enable.

[0]: Disable.

[1]: Enable.

BDF: Battery detection flag.

[0]: Low Battery.

[1]: High Battery.

23.5 FUNCTION DESCRIPTION

A8125M0 has a built-in battery detector to check supply voltage (VDD_IO pin). Battery detect function has a control register. User can select Battery detection threshold by setting BVT[2:0], and the detecting range is 2.0V ~ 2.7V in 8 levels. Enable Battery detect function by setting BDS = 1, and MCU read bit BDF (Battery detection flag) to detect voltage condition. If Battery voltage less than threshold, BDF will output low; otherwise BDF will output high.

23.6 PROCEDURE

Below is the procedure to detect low voltage input (ex. battery detection threshold 2.1V):

1. Set standby or PLL mode.
2. Set BDV[2:0](0x50000000) = [001] and enable BDE = 1.
3. After 5 us, BDE is auto clear.
4. MCU reads BDF.
5. If VDD_IO pin voltage $\geq 2.1V$, BDF = 1 (battery high); otherwise BDF = 0 (battery low). Then back to step (2).

24. Flash memory controller

24.1 Flash controller operations

INF Truth Table

Mode	INF = Logic 1	INF= Logic 0
Read	Read the information page	Read the main memory block
Write	Write the information page	Write the main memory block
Program	Program the information page	Program the main memory block
Page Erase	Erase the information page	Erase the main memory block
Sector Erase	Erase the information page	Erase the main memory block
Mass Erase	Erase both main memory block and information page.	Erase the main memory block

Page Write

The Page Write time (T_{WR}) also includes T_{BUSY} and the internal Program cycle. During this period, the internal Program cycle will start when RBB is set at logic 0 after T_{BUSY} . This operation allows writing page function to change data from "1" to "0". The data of the selected page need to be erased by performing Page Erase, Sector Erase, or Mass Erase operation before Page Write operation. The data can be written into Assembly Buffer separately, and then be written in main memory block. The writing sequence allows up to 32 X 32 bits in a page written at the same time.

The written page cannot be re-written if Erase operation is not performed in advance; even only partial data in the selected page are written. For example, 8 X 32 bits are written into the selected page by using Page Write command. After this command has been done, the rest 24 X 32 bits cannot be written into the same selected page if Page Erase command is not performed in advance. It is suggested to use Page Write command to change whole page data.

Page/Sector/Mass Erase

Since in Page Write operation, the data will be changed to "0", Erase operations should be applied before the Page Write operation to reset all the data back to "1". The whole data in a page, a sector or all the main memory can be erased at a time by performing Page Erase, Sector Erase, or Mass Erase sequences accordingly.

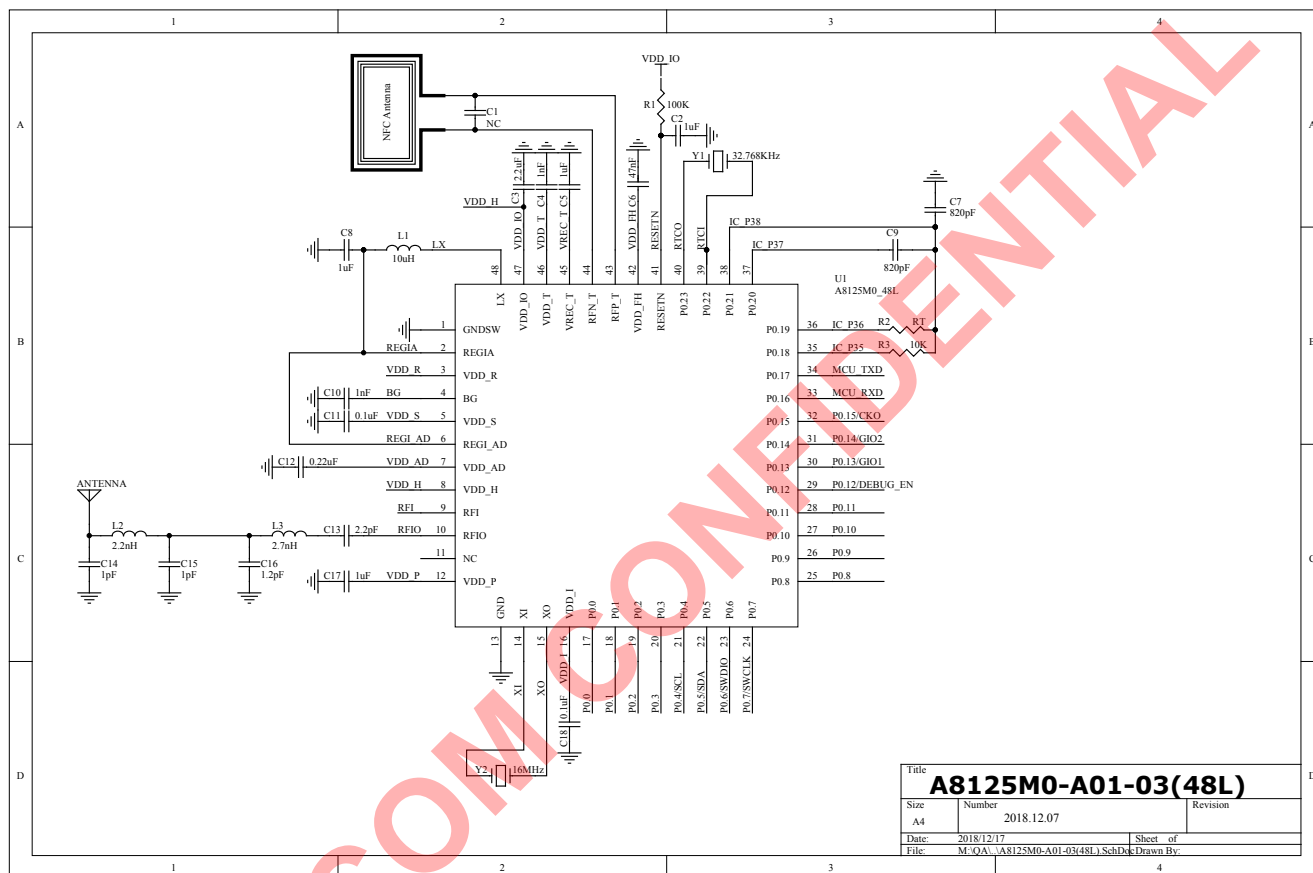
Ready/Busy Port (RBB) During a Write, Program, Erase Cycle

The RBB port provides status of internal operations (Page Write, Page Program, Page Erase, Sector Erase, Mass Erase, Power On Reset, and Low Standby MODEs). Users can know whether the eFlash macro is ready to serve next command by monitoring the RBB. Any other commands are ignored while the RBB is at logic 0 state.

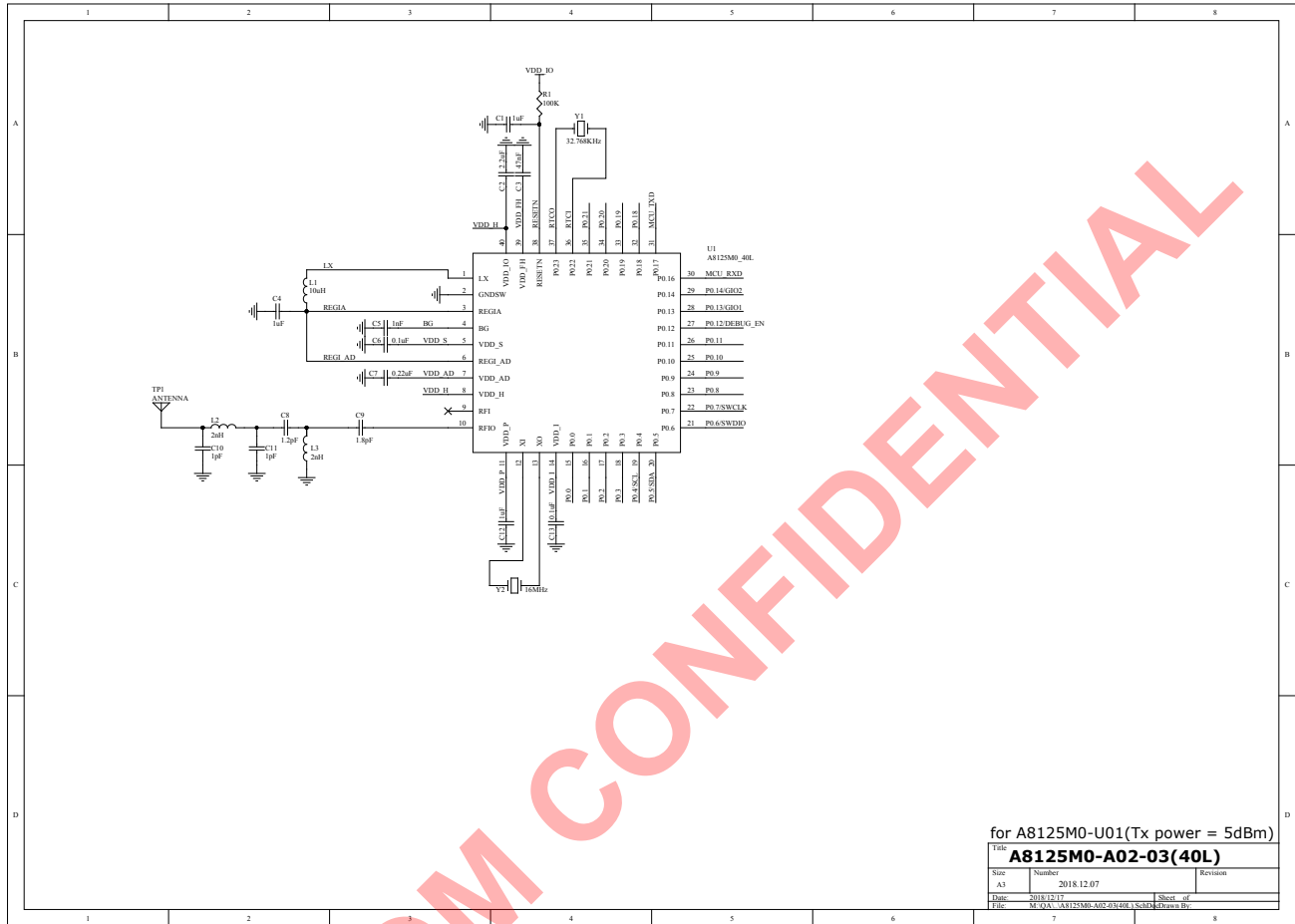
25. Application circuit

Below are AMICCOM's ref. design circuits. For more details, please contact AMICCOM's FAE for more details.

A8125M0 QFN48 6x6 Package



A8125M0 QFN40 5x5 Package



26. Abbreviations

ADC	Analog to Digital Converter
AIF	Auto IF
FC	Frequency Compensation
AGC	Automatic Gain Control
BER	Bit Error Rate
BW	Bandwidth
CD	Carrier Detect
CHSP	Channel Step
CRC	Cyclic Redundancy Check
CODEC	Coder and Decoder
DAC	Digital to Analog Converter
DC	Direct Current
FEC	Forward Error Correction
FIFO	First in First out
FSK	Frequency Shift Keying
ID	Identifier
ICE	In Circuit Emulator
IF	Intermediate Frequency
ISM	Industrial, Scientific and Medical
LO	Local Oscillator
MCU	Micro Controller Unit
PFD	Phase Frequency Detector for PLL
PLL	Phase Lock Loop
POR	Power on Reset
PWM	Pulse width modulation
RX	Receiver
RXLO	Receiver Local Oscillator
RSSI	Received Signal Strength Indicator
SPI	Serial to Parallel Interface
SYCK	System Clock for digital circuit
TX	Transmitter
TXRF	Transmitter Radio Frequency
VCO	Voltage Controlled Oscillator
XOSC	Crystal Oscillator
XREF	Crystal Reference frequency
XTAL	Crystal

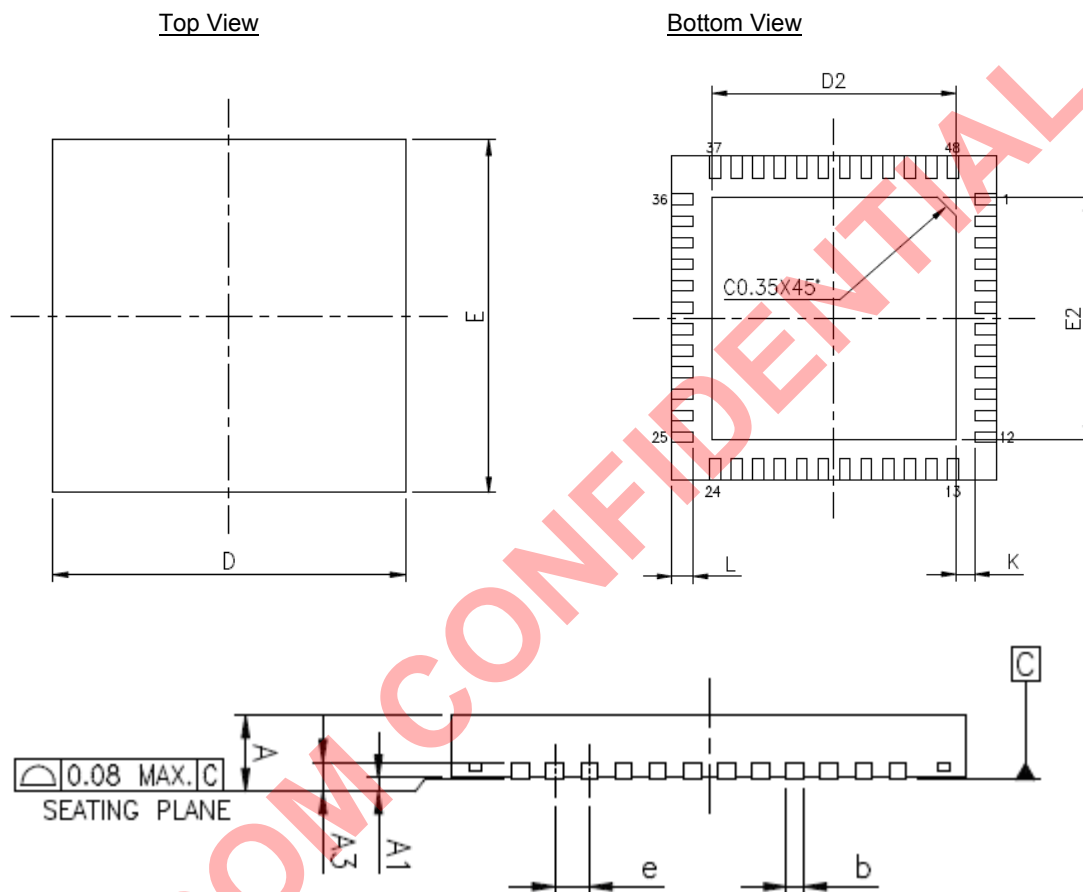
27. Ordering Information

Part No.	Package	Units Per Reel / Tray
A81U25F7101AQ6C/Q	QFN6x6, Pb Free, Tape & Reel, -40°C ~ 85°C	3K
A81U25F7101AQ6C	QFN6x6, Pb Free, Tray, -40°C ~ 85°C	490EA
A81U25F7101AQ5A/Q	QFN5x5, Pb Free, Tape & Reel, -40°C ~ 85°C	3K
A81U25F7101AQ5A	QFN5x5, Pb Free, Tray, -40°C ~ 85°C	490EA

28. Package Information

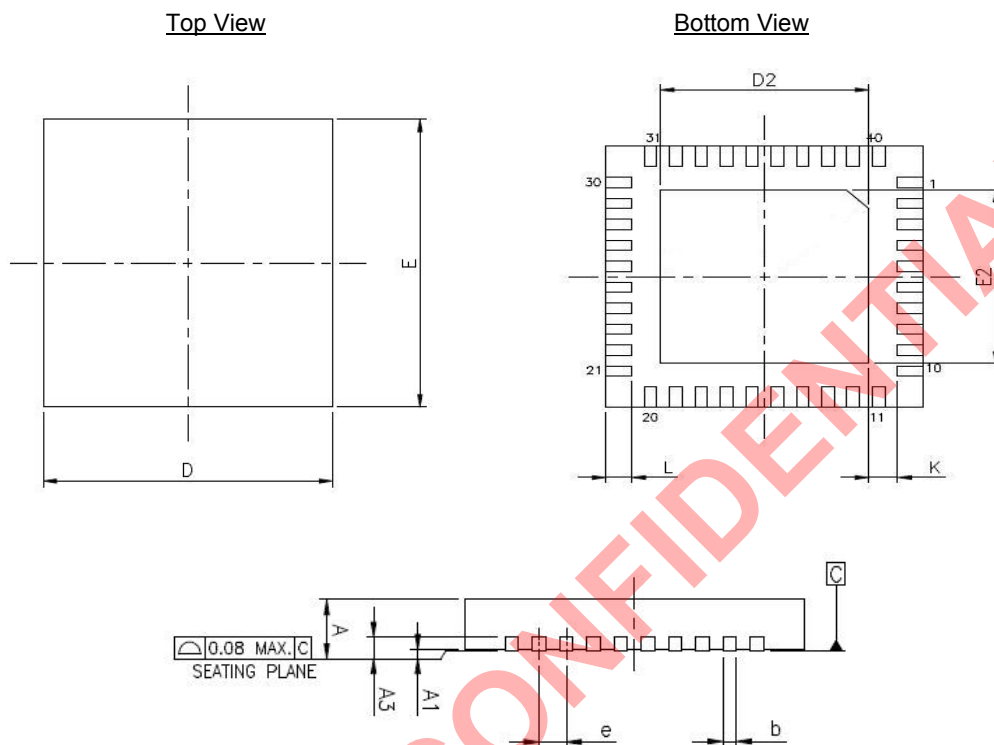
QFN6*6 48L Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.028	0.030	0.031	0.7	0.75	0.8
A ₁	0	0.001	0.002	0.00	0.02	0.05
A ₃	0.009 REF.			0.23REF.		
b	0.006	0.008	0.010	0.15	0.2	0.25
D	0.240			6.1 BSC		
D ₂	0.146	0.177	0.179	3.70	4.50	4.55
E	0.240			6.1BSC		
E ₂	0.146	0.177	0.179	3.70	4.50	4.55
e	0.016BSC			0.4BSC		
L	0.013	0.016	0.020	0.32	0.4	0.50
K	0.008	-	-	0.2	-	-

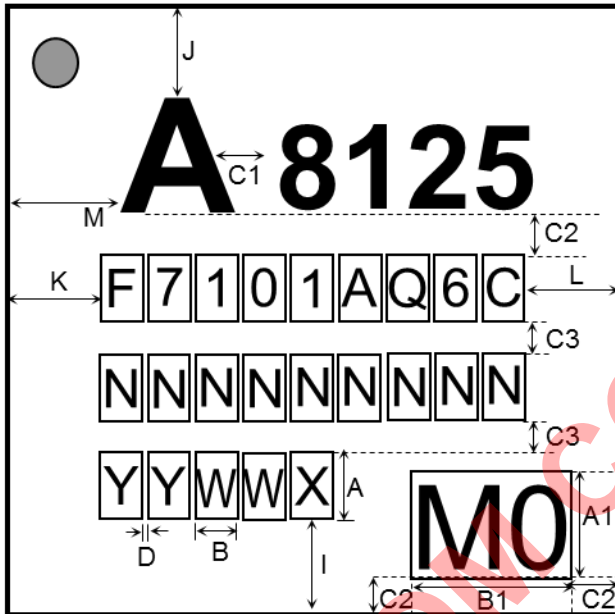
QFN5*5 40L Outline Dimensions



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.028	0.030	0.031	0.70	0.75	0.80
A ₁	0.000	0.001	0.002	0.00	0.02	0.05
A ₃	0.008 REF			0.20 REF		
b	0.006	0.008	0.010	0.15	0.20	0.25
D	0.194	-	0.200	4.924	-	5.1
D ₂	0.126	-	0.138	3.20	-	3.50
E	0.194	-	0.200	4.924	-	5.1
E ₂	0.126	-	0.138	3.20	-	3.50
e	0.016			0.40		
L	0.013	0.016	0.019	0.324	0.40	0.5
k	0.008			0.2		

29. Top Marking Information

- Part No. : A81U25F7101AQ6C
- Pin Count : 48
- Package Type : QFN
- Dimension : 6*6 mm
- Mark Method : Laser Mark
- Character Type : Arial



❖ CHARACTER SIZE : (Unit in mm)

A : 0.65 A1 : 0.75
 B : 0.45 B1 : 1.10
 C1 : 0.3 C2 : 0.4 C3 : 0.3
 D : 0.03
 M : 1.5

YYWW

: DATECODE

X

: PKG HOUSE ID

NNNNNNNNNN

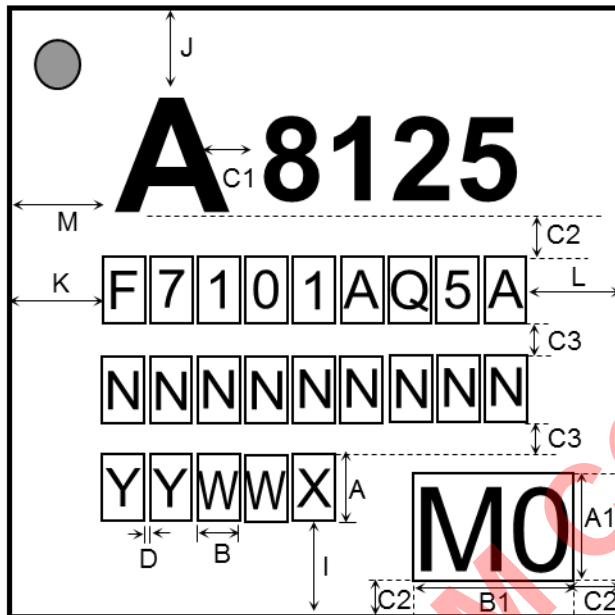
: LOT NO.
 (max. 9 characters)

I=J
 K=L

0.90
 A
 0.78

0.75
 8125
 1.70

- Part No. : A81U25F7101AQ5A
- Pin Count : 40
- Package Type : QFN
- Dimension : 5*5 mm
- Mark Method : Laser Mark
- Character Type : Arial



❖ CHARACTER SIZE : (Unit in mm)

A : 0.55

B : 0.36

C1 : 0.25 C2 : 0.3 C3 : 0.2

D : 0.03

M : 1.5

YYWW

: DATECODE

X

: PKG HOUSE ID

NNNNNNNNNN

: LOT NO.
(max. 9 characters)

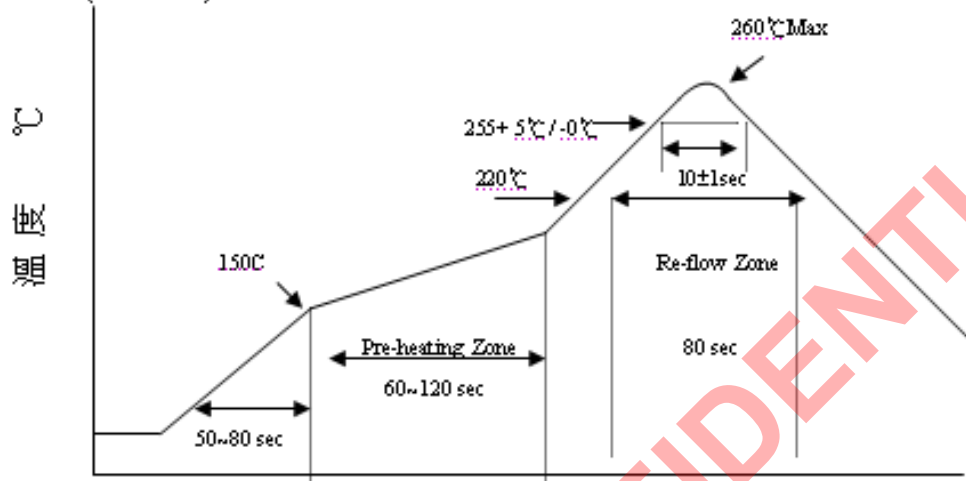
I=J
K=L

0.80
A
0.68

0.65
8125
1.6

30. Reflow Profile

LEAD FREE (GREEN) PROFILE :

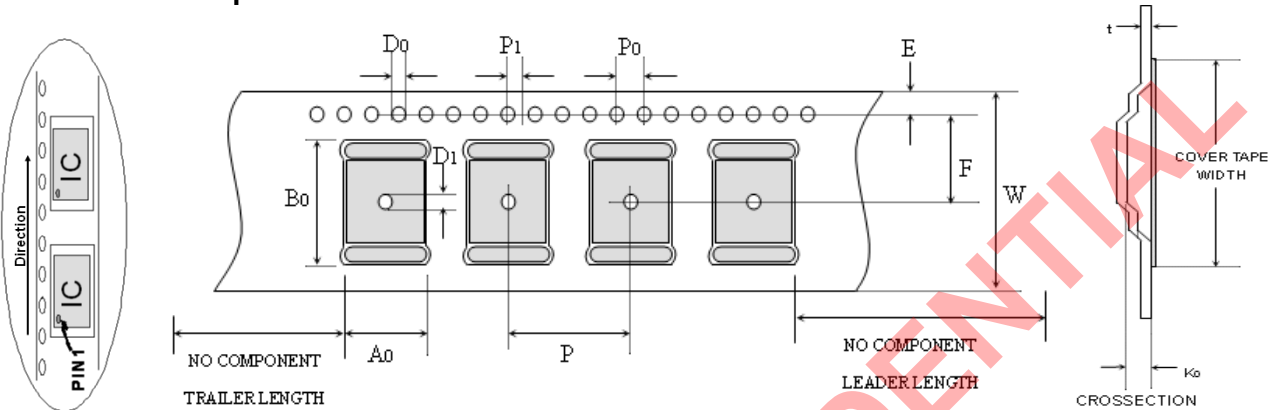


Actual Measurement Graph



31. Tape Reel Information

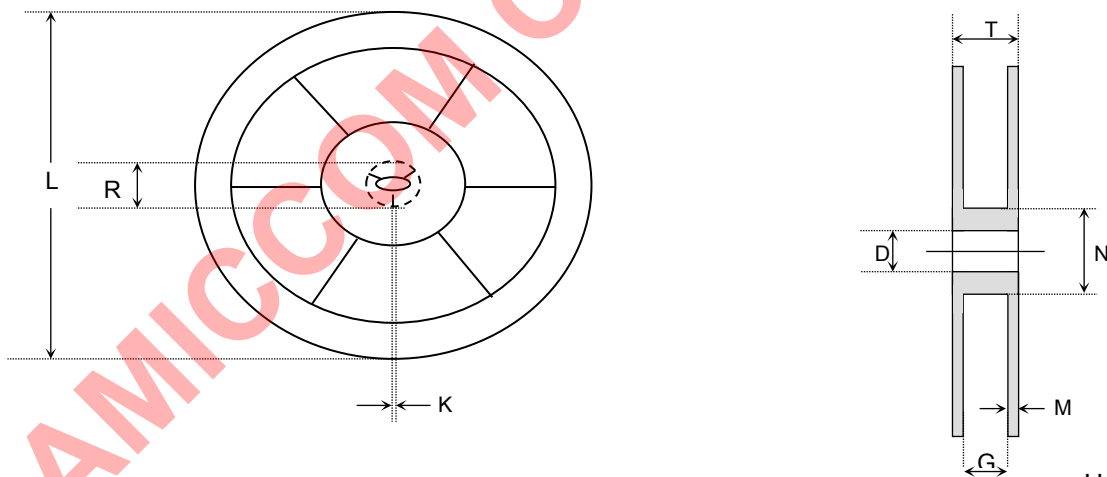
Cover / Carrier Tape Dimension



Unit: mm

TYPE	P	A0	B0	P0	P1	D0	D1	E	F	W	K0	t	Cover tape width
QFN 5*5	8±0.1	5.25±0.1	5.25±0.1	4±0.2	2±0.1	1.5±0.1	1.5	1.75±0.1	5.5±0.05	12±0.3	1.25±0.1	0.3±0.05	9.3±0.1
QFN 6*6	12±0.1	6.3±0.1	6.3±0.1	4±0.2	2±0.1	1.5±0.1	1.5±0.5	1.75±0.1	7.5±0.1	16±0.3	1.15±0.2	0.3±0.05	13.3±0.1

REEL DIMENSIONS



Unit: mm

TYPE	G	N	M	D	K	L	R
QFN5*5	12.9±0.5	102 REF±2.0	2.3±0.2	13.15±0.35	2.0±0.5	330±3.0	19.6±2.9
QFN6*6	17±0.5	102 REF±2.0	2.3±0.2	13.15±0.35	2.0±0.5	330±3.0	19.6±2.9

32. Product Status

Data Sheet Identification	Product Status	Definition
Objective	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification	Noted Full Production	This data sheet contains the final specifications. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by AMICCOM. The data sheet is printed for reference information only.

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